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OKUMOTO et al.

(54) **THIN-FILM TRANSISTOR DEVICE AND METHOD FOR MANUFACTURING SAME, ORGANIC ELECTROLUMINESCENT DISPLAY ELEMENTS AND ORGANIC ELECTROLUMINESCENT DISPLAY DEVICE**

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(52) **U.S. Cl.**

CPC ***H01L 27/32*** (2013.01); ***H01L 27/1214*** (2013.01); ***H01L 29/66765*** (2013.01)

USPC **257/40**; 257/59; 438/158

(57) **ABSTRACT**

A thin film transistor element is formed in each of a first aperture and a second aperture defined by partition walls, which further define a third aperture that is adjacent to the first aperture with a gap therebetween and is located in a direction, from the first aperture, differing from a direction of the second aperture. In plan view, at a bottom portion of the first aperture, a center of area of a liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the third aperture, and at a bottom portion of one of the first and second apertures, a center of area of a liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the other one of the first and second apertures.

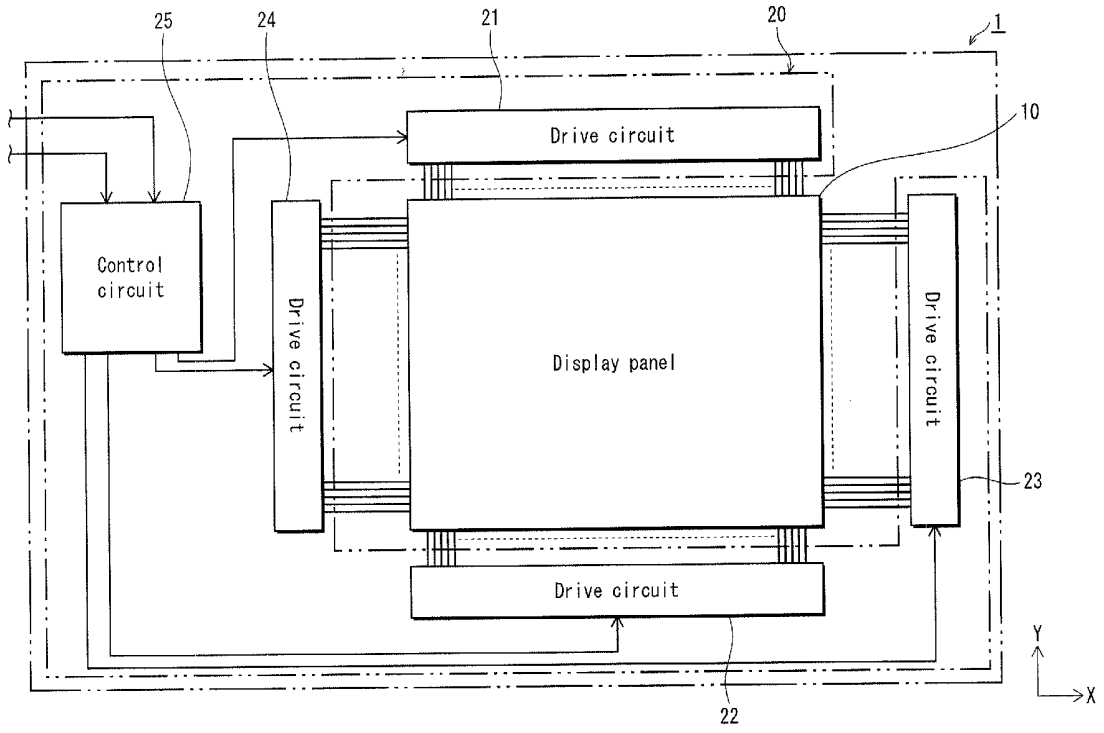


FIG. 1

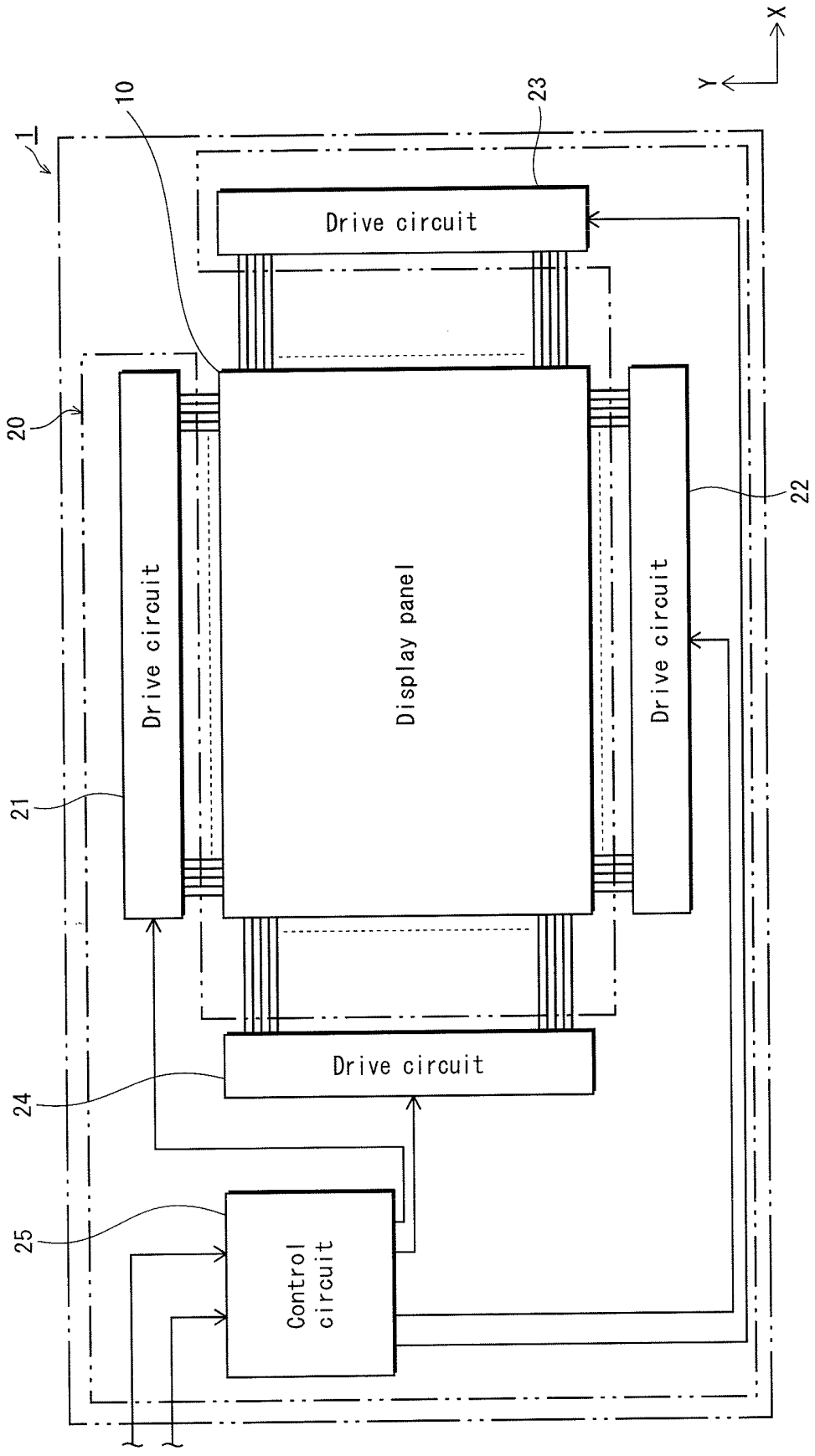
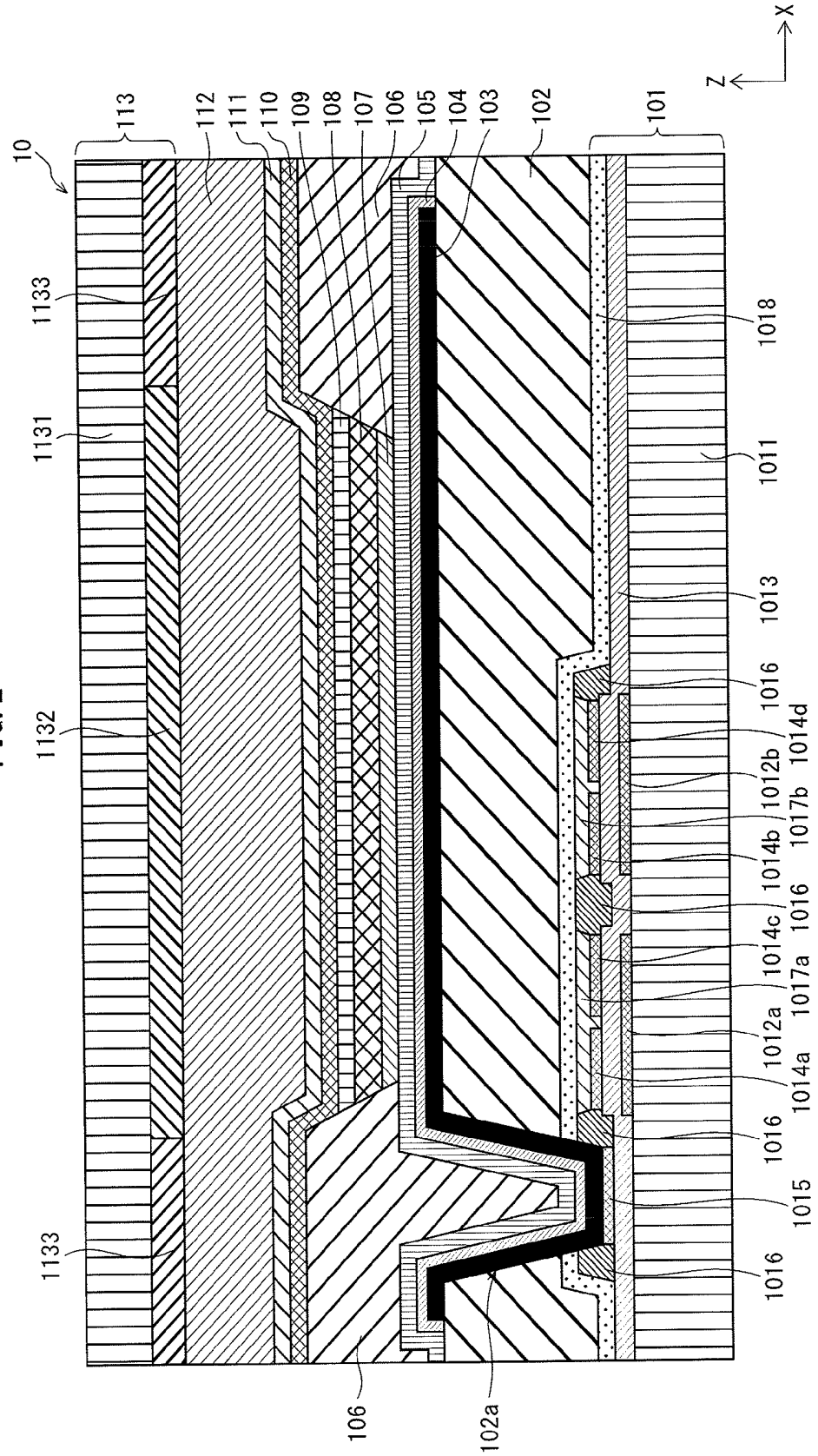

X
Y
1
10
23
Drive circuit
20
Drive circuit
Display panel
Drive circuit
22
21
Drive circuit
24
25
Control circuit

FIG. 2


X
Z
10
113
112
111
110
109
108
107
106
105
104
103
102
101
1133
1131
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1133
1018
1011
1013
1016
1014d
1012b
1017b
1014b
1016
1014c
1017a
1012a
1014a
1016
1015
1016
106
102a

FIG. 3

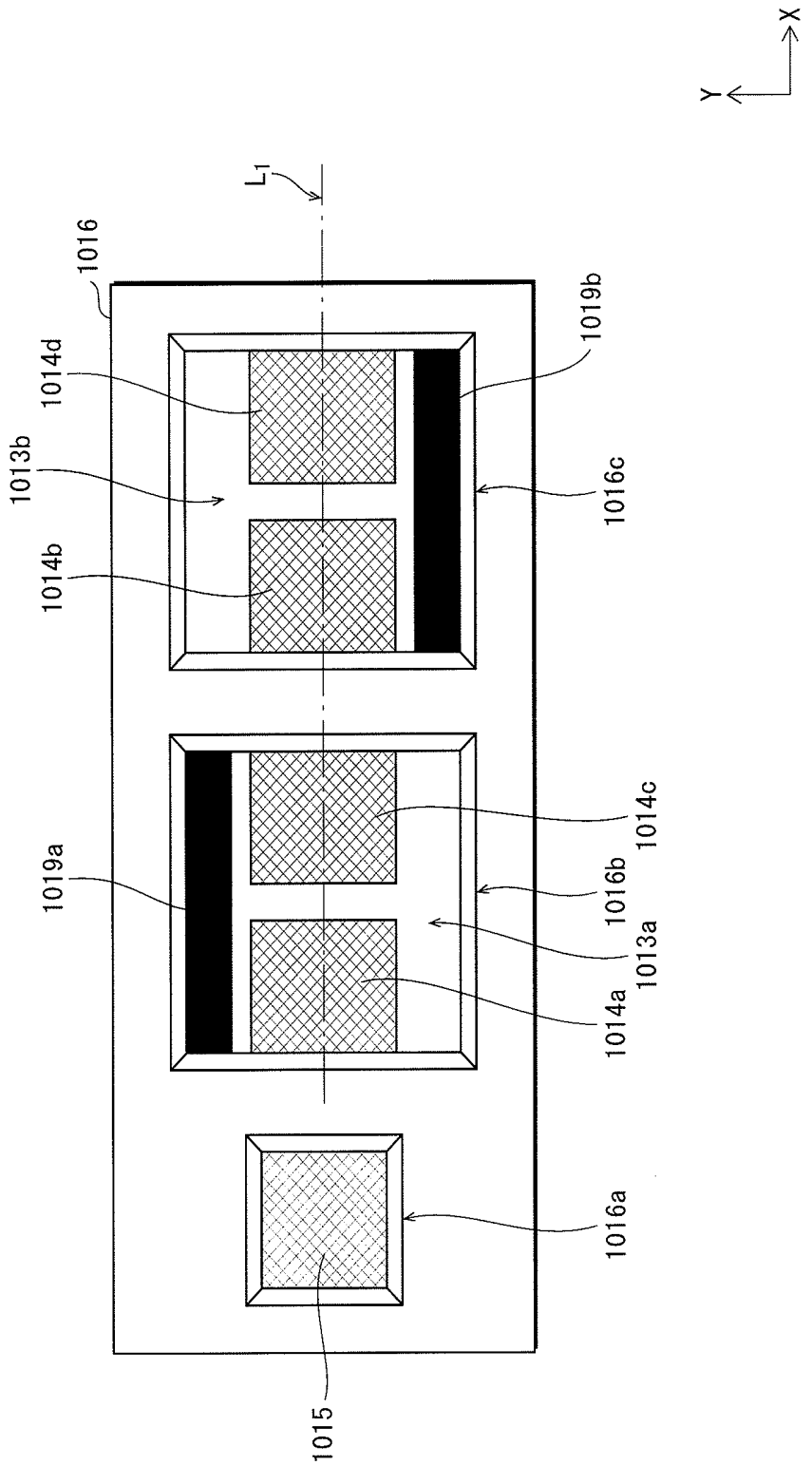

X
Y
L_1
1016
1014d
1019b
1013b
1016c
1014b
1014c
1019a
1016b
1013a
1014a
1016a
1015

FIG. 4A

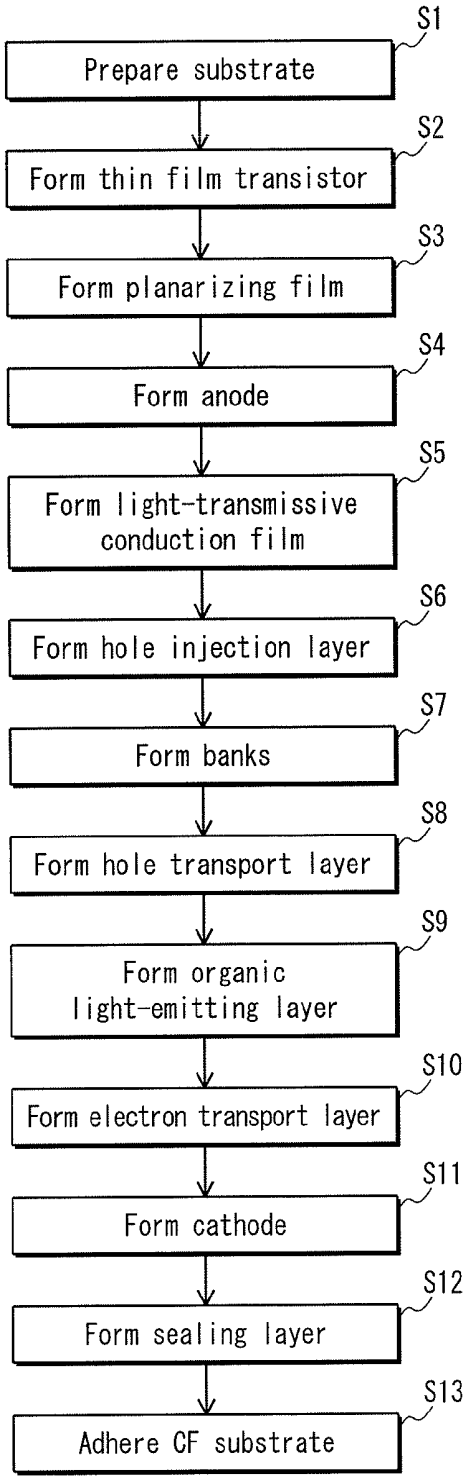
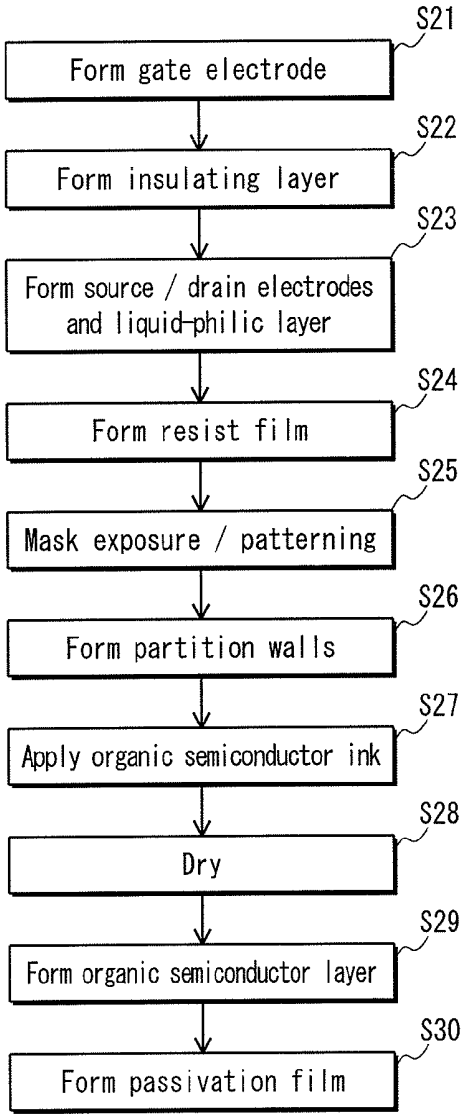

S1
Prepare substrate
S2
Form thin film transistor
S3
Form planarizing film
S4
Form anode
S5
Form light-transmissive conduction film
S6
Form hole injection layer
S7
Form banks
S8
Form hole transport layer
S9
Form organic light-emitting layer
S10
Form electron transport layer
S11
Form cathode
S12
Form sealing layer
S13
Adhere CF substrate

FIG. 4B


S21
Form gate electrode
S22
Form insulating layer
S23
Form source / drain electrodes and liquid-philic layer
S24
Form resist film
S25
Mask exposure / patterning
S26
Form partition walls
S27
Apply organic semiconductor ink
S28
Dry
S29
Form organic semiconductor layer
S30
Form passivation film

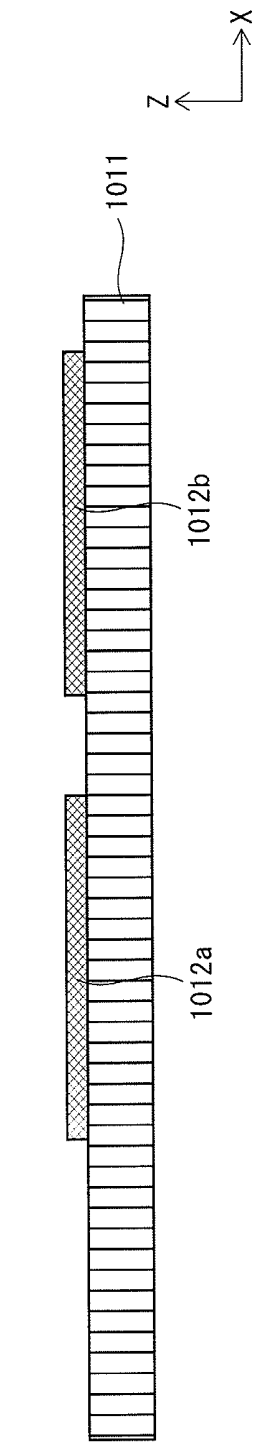


FIG. 5A

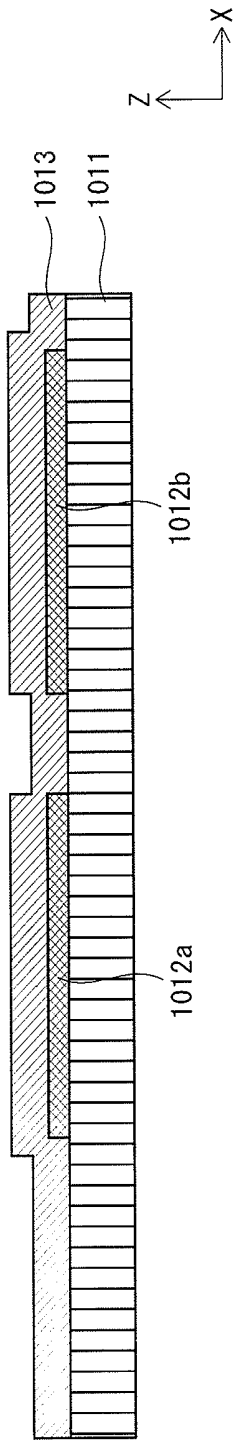


FIG. 5B

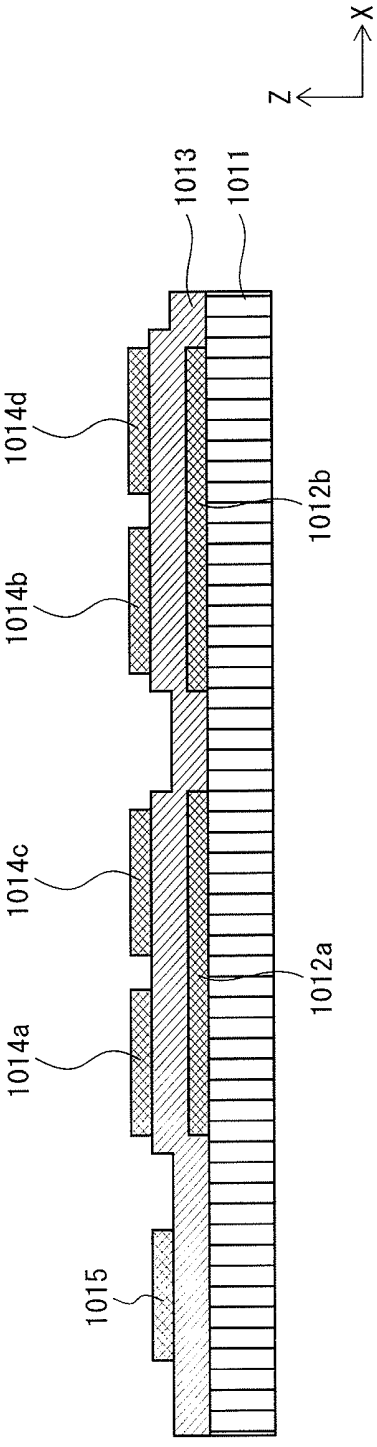


FIG. 5C

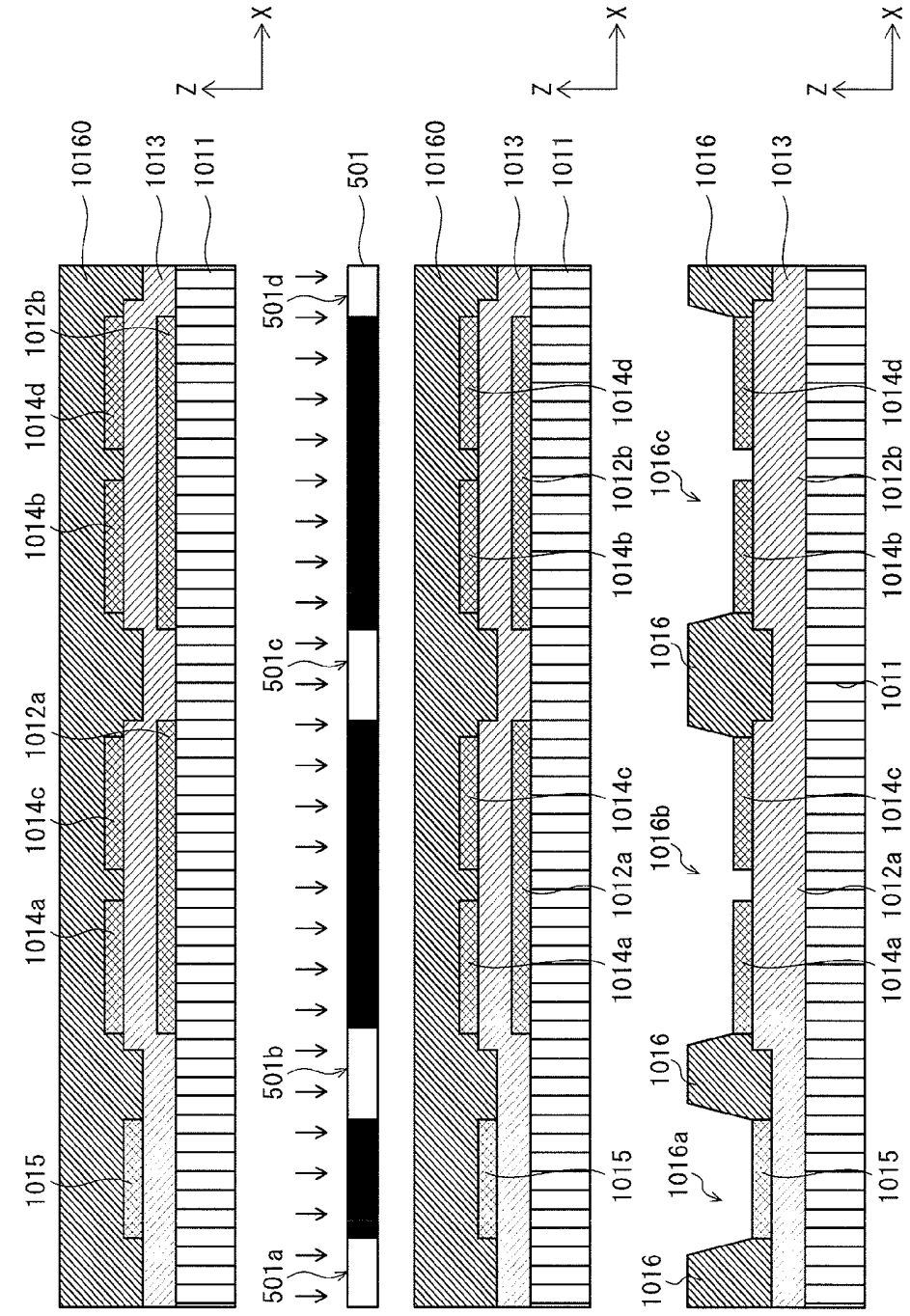


FIG. 6A

FIG. 6B

FIG. 6C

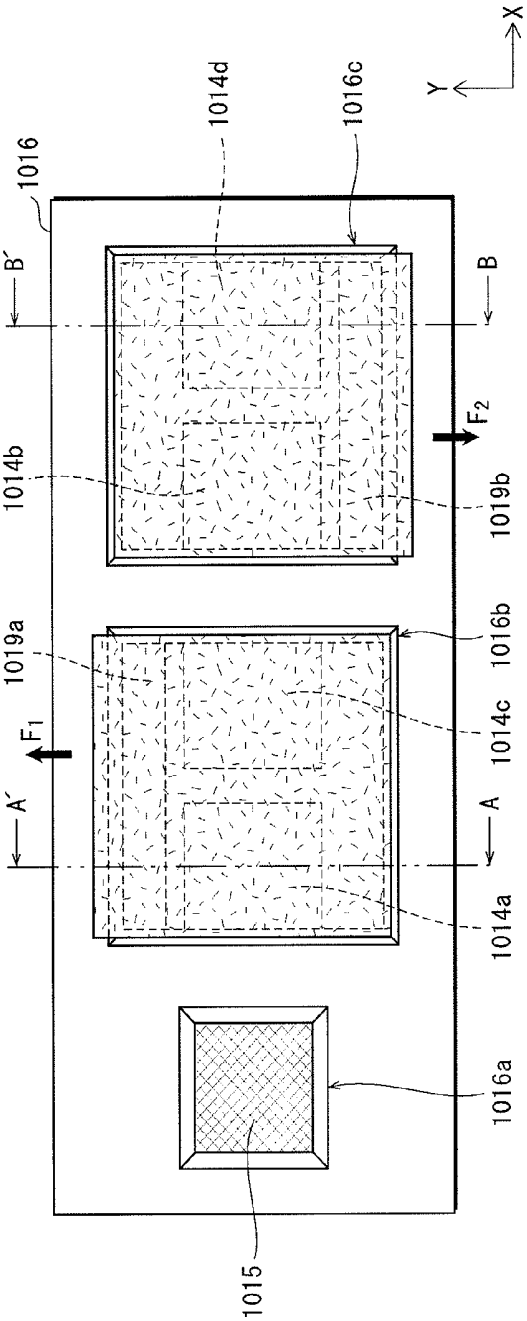


FIG. 7A

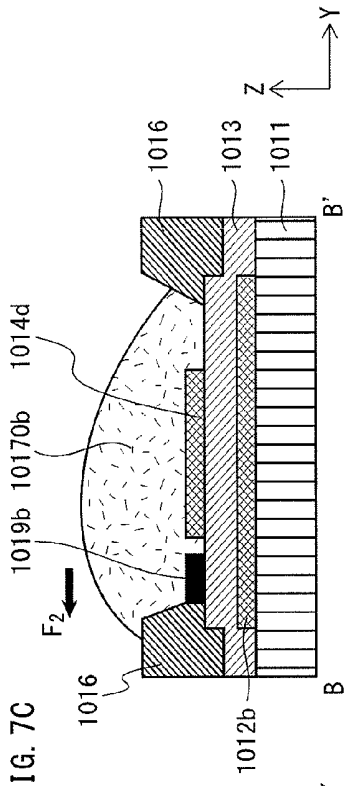


FIG. 7C

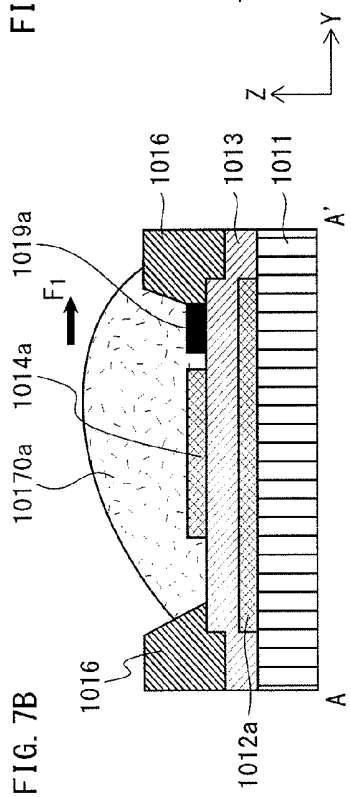


FIG. 7B

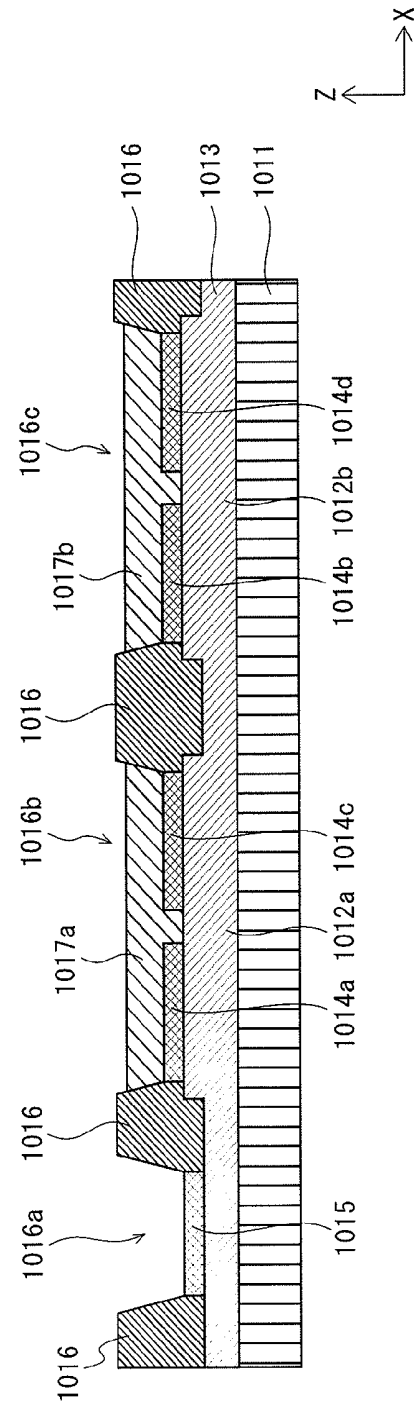

Z
X
1016
1013
1011
1016c
1014d
1012b
1017b
1014b
1016
1016b
1014c
1012a
1017a
1014a
1016
1015
1016a
1016

FIG. 8A

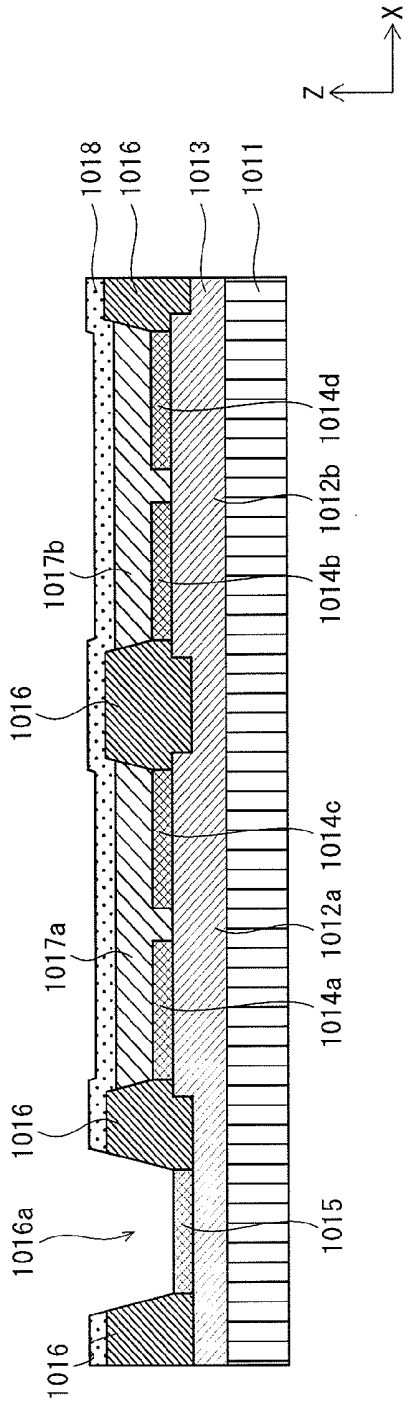

Z
X
1018
1016
1013
1011
1014d
1012b
1017b
1014b
1016
1014c
1012a
1017a
1014a
1016
1015
1016a
1016

FIG. 8B

FIG. 9A

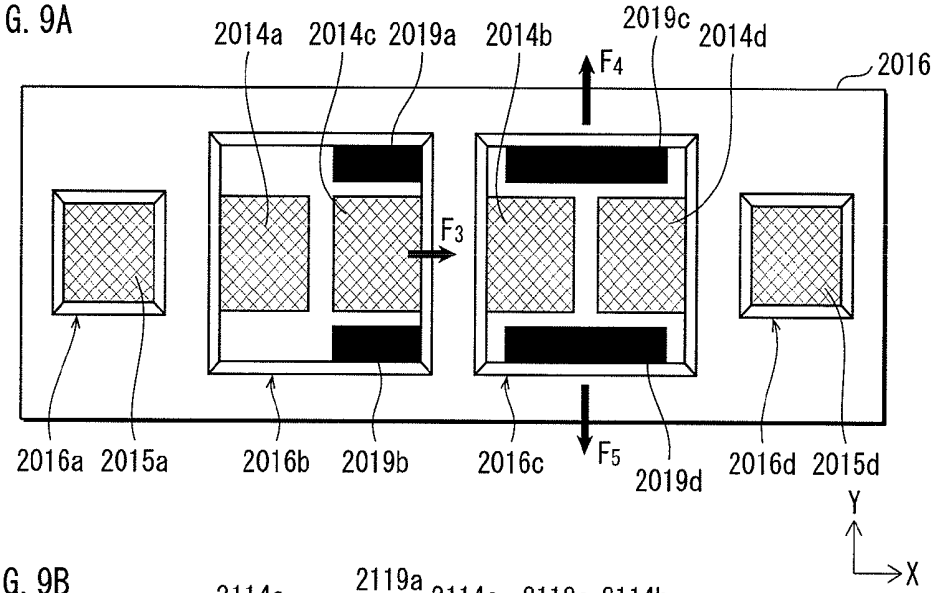


FIG. 9B

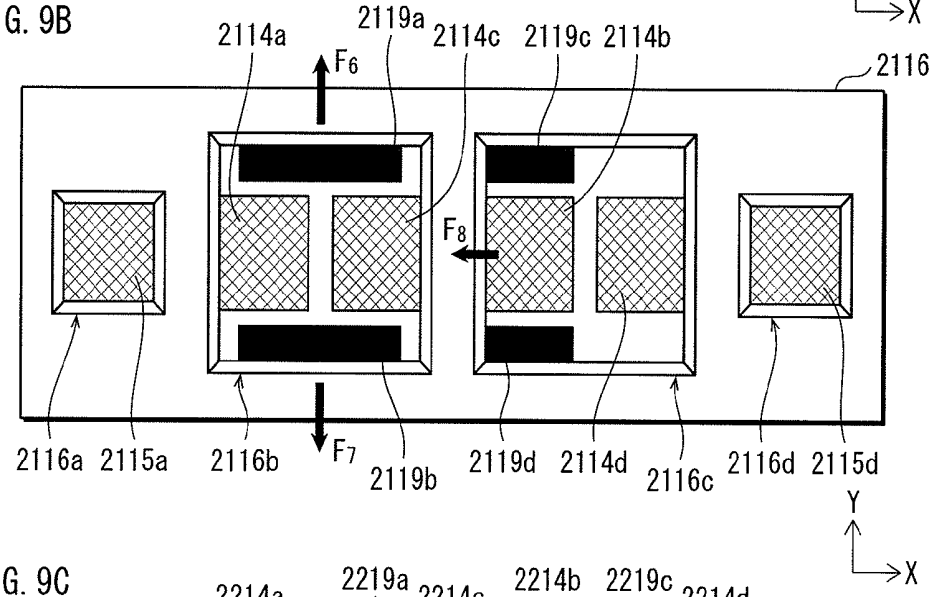


FIG. 9C

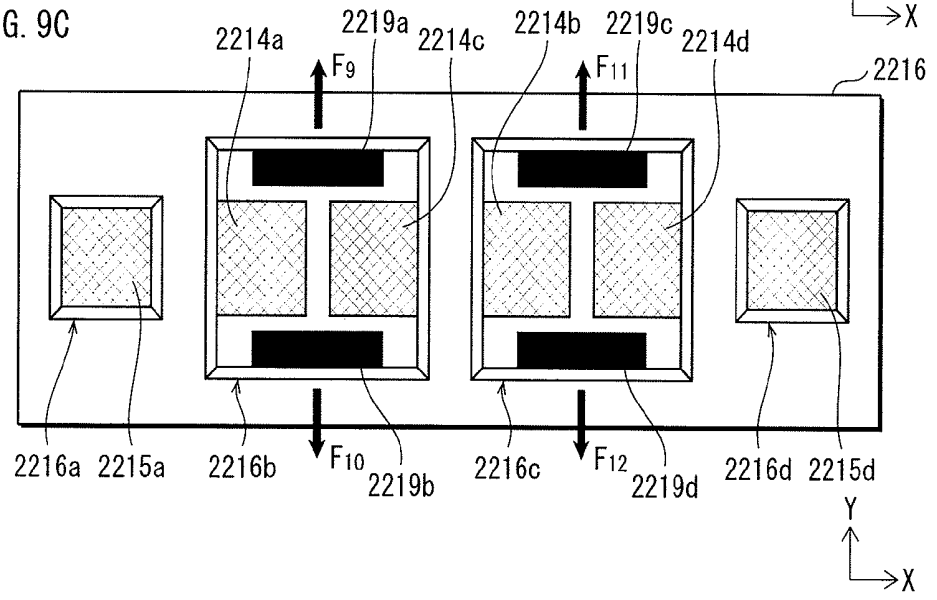


FIG. 10A

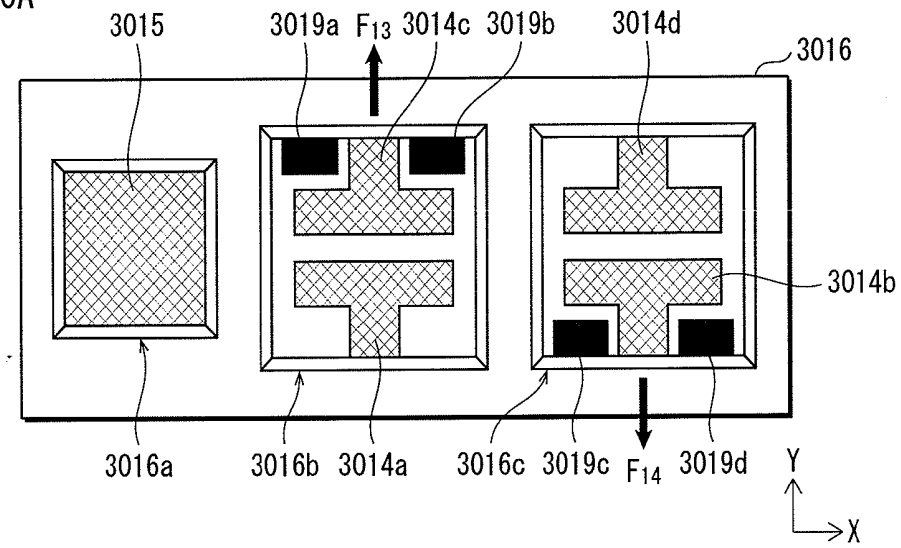


FIG. 10B

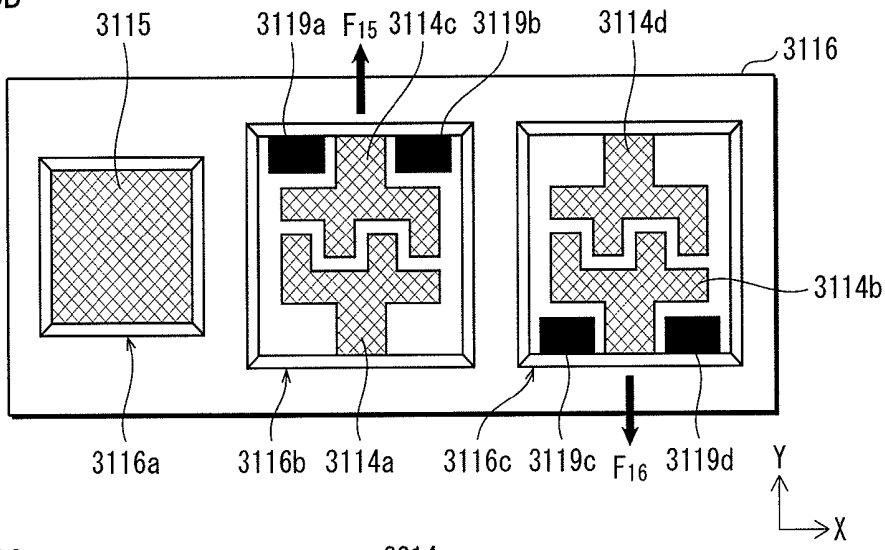


FIG. 10C

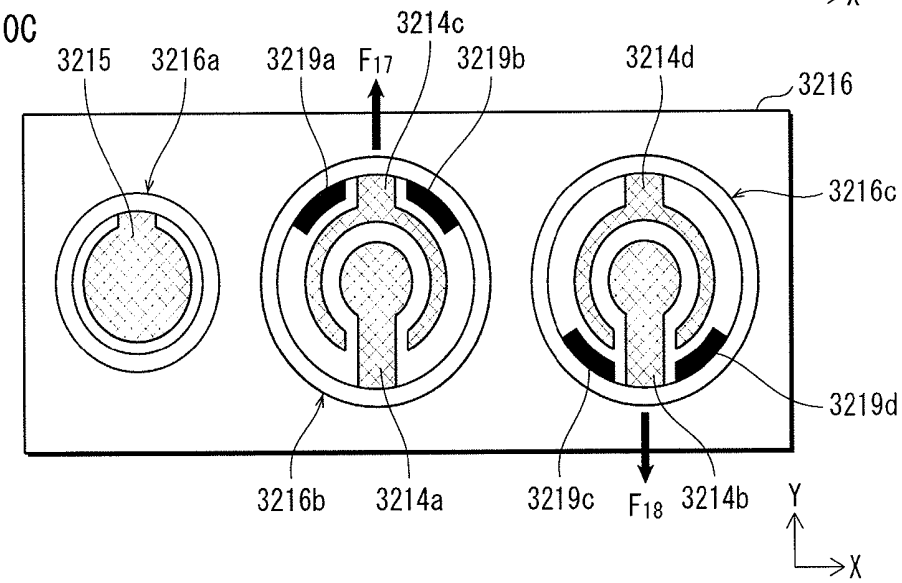


FIG. 11A

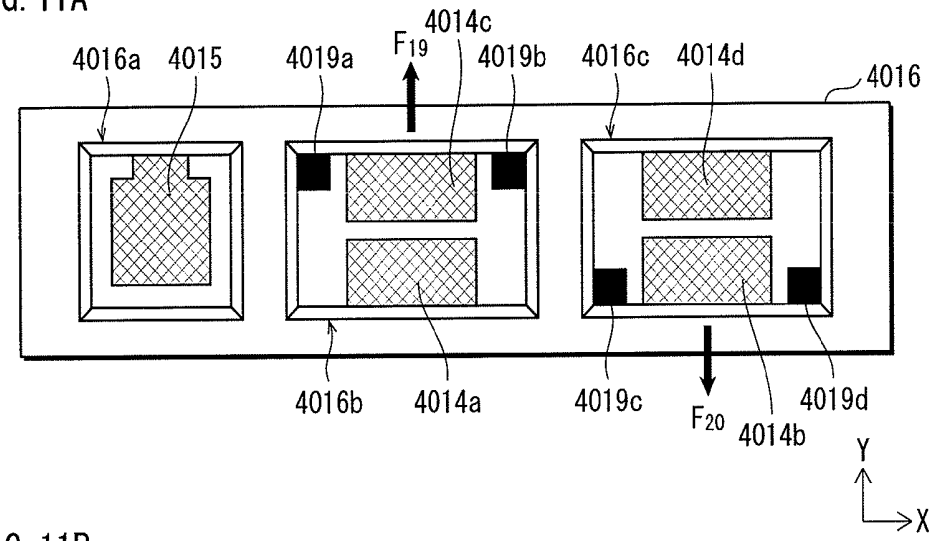


FIG. 11B

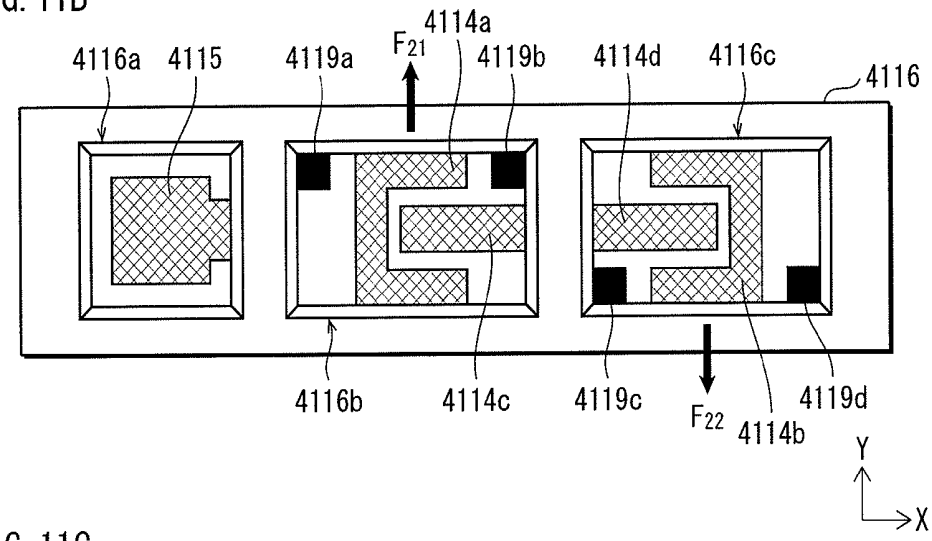


FIG. 11C

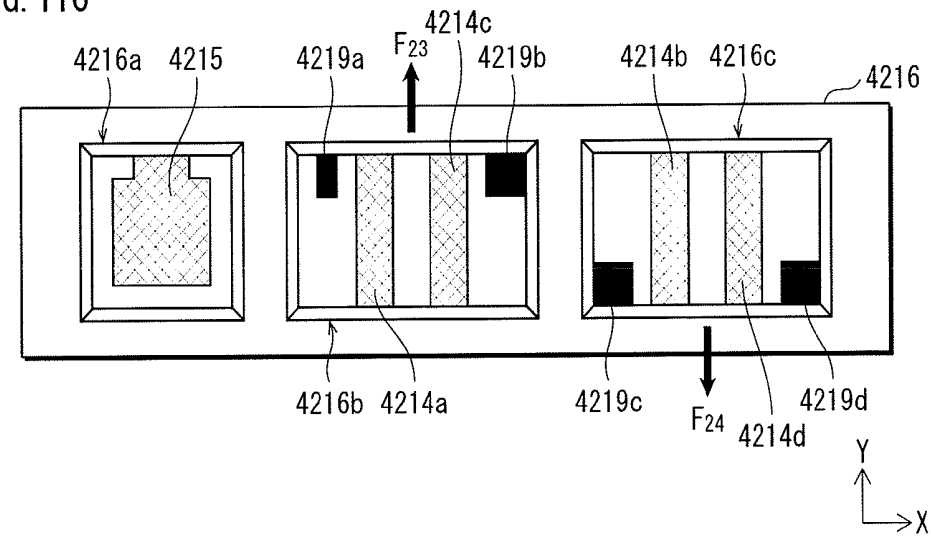


FIG. 12A

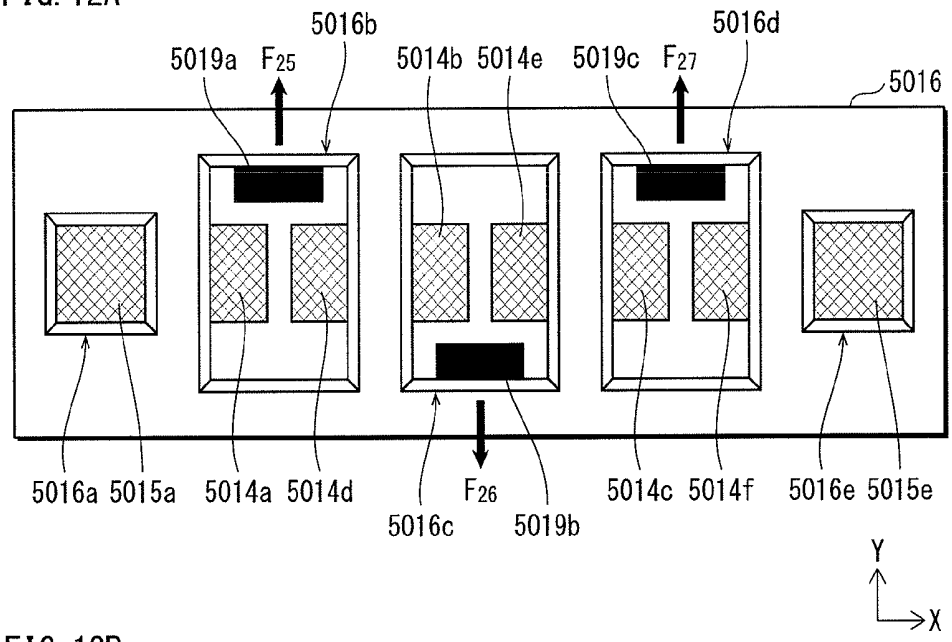


FIG. 12B

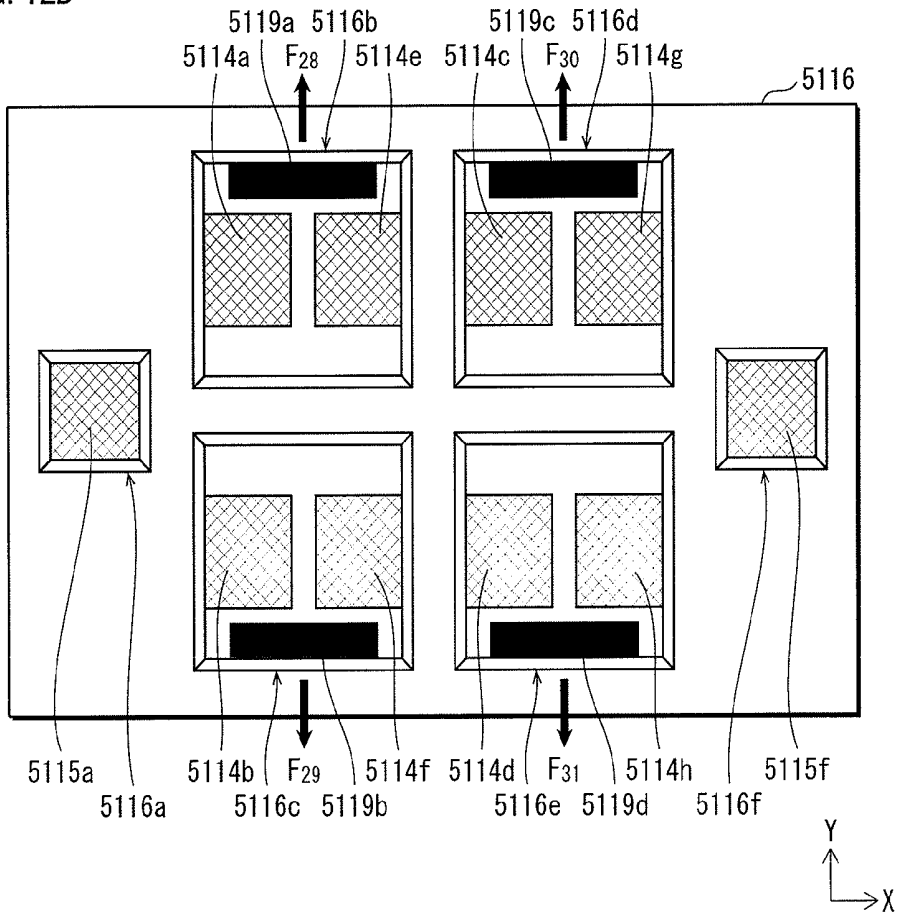


FIG. 13

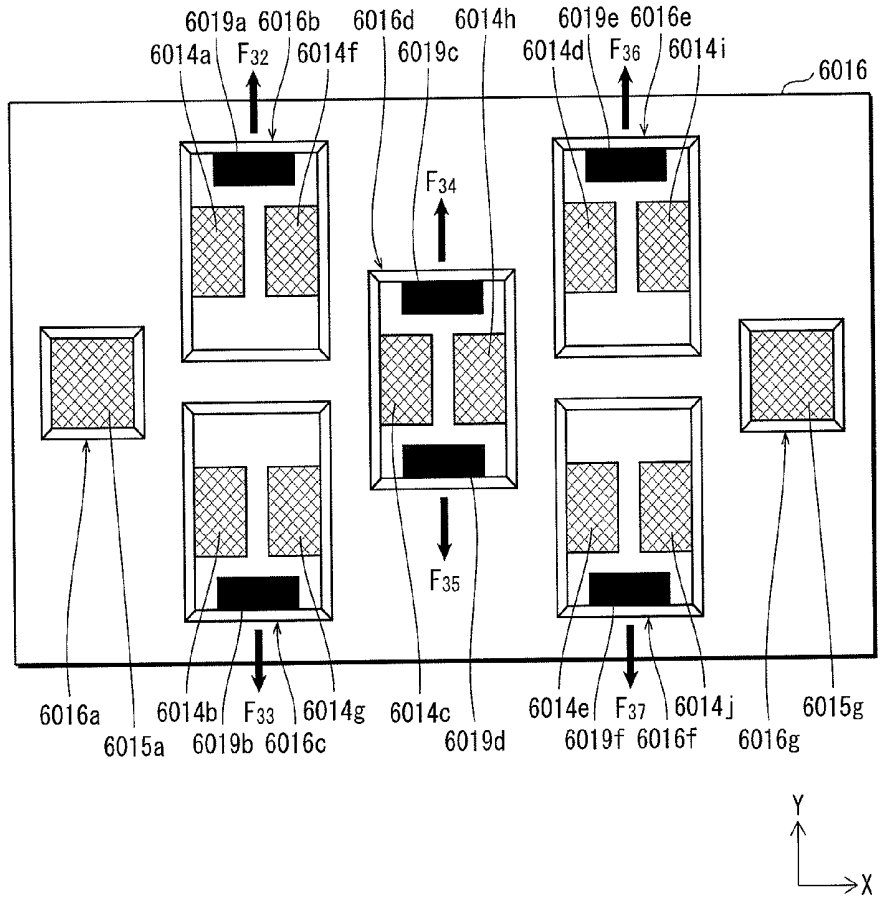

6019a
6016b
6016d
6014h
6019e
6016e
6014a
F32
6014f
6019c
6014d
F36
6014i
6016
F34
F35
6016a
6015a
6014b
F33
6019b
6016c
6014g
6014c
6019d
6014e
F37
6019f
6016f
6014j
6016g
6015g
Y
X

FIG. 14A

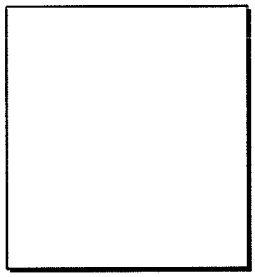


FIG. 14B

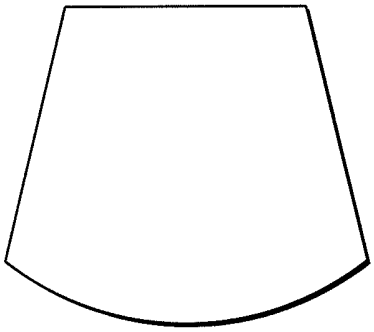
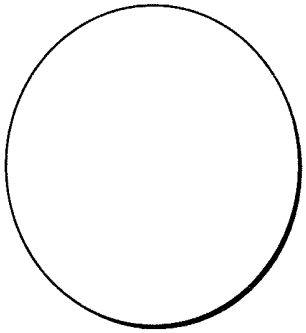
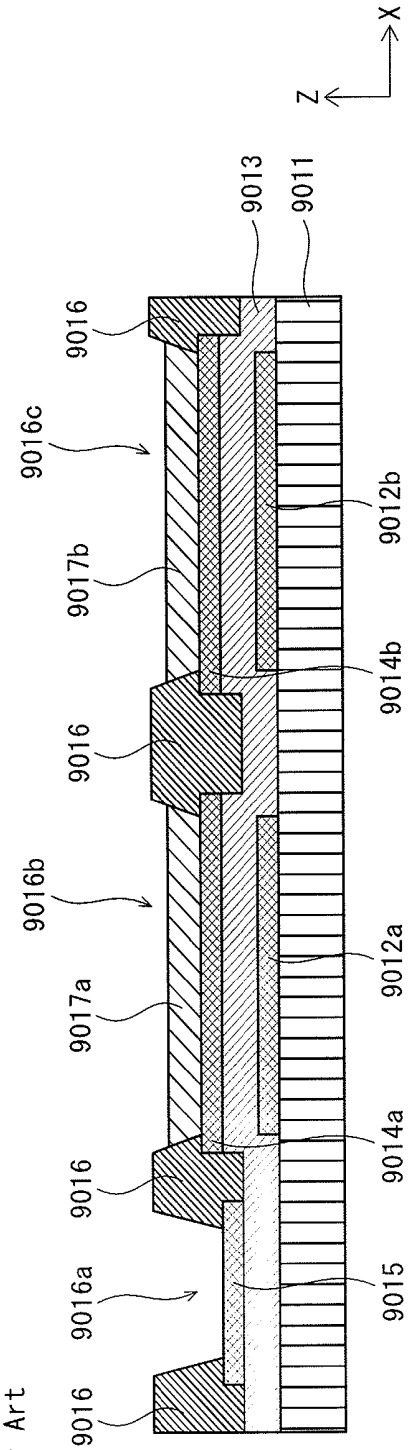


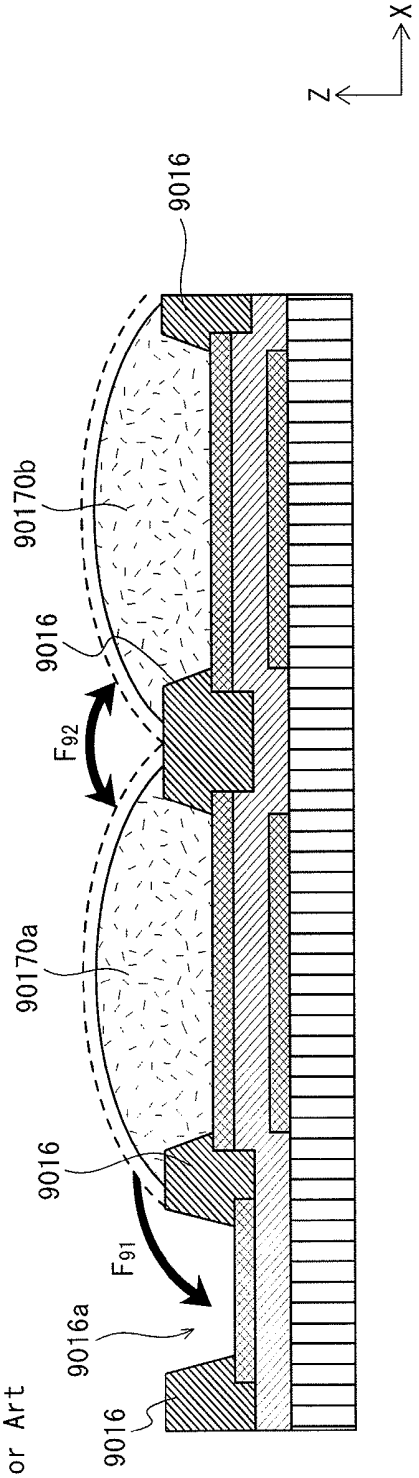
FIG. 14C





Prior Art

FIG. 15A



Prior Art

FIG. 15B

THIN-FILM TRANSISTOR DEVICE AND METHOD FOR MANUFACTURING SAME, ORGANIC ELECTROLUMINESCENT DISPLAY ELEMENTS AND ORGANIC ELECTROLUMINESCENT DISPLAY DEVICE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This is a continuation application of PCT Application No. PCT/JP2012/005995 filed Sep. 21, 2012, designating the United States of America, the disclosure of which, including the specification, drawings and claims, is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to a thin film transistor device and a manufacturing method thereof, an organic EL display element, and an organic EL display device.

DESCRIPTION OF THE RELATED ART

[0003] In liquid crystal display panels and organic EL display panels, control of light emission is performed in units of subpixels. To make this possible, thin film transistor devices are used in liquid crystal display panels and organic EL display panels. A thin film transistor device includes a thin film transistor (TFT) element formed for each subpixel. In particular, development is in progress of a thin film transistor device that includes a semiconductor layer formed by using organic semiconductor material.

[0004] As illustrated in FIG. **15**A, a conventional organic TFT device includes, for instance: a substrate **9011**; gate electrodes **9012***a*, **9012***b*; an insulating layer **9013**; source electrodes **9014***a*, **9014***b*; drain electrodes (undepicted); and organic semiconductor layers **9017***a*, **9017***b*. The gate electrodes **9012***a*, **9012***b*, the insulating layer **9013**, the source electrodes **9014***a*, **9014***b*, the drain electrodes, and the organic semiconductor layers **9017***a*, **9017***b* are formed by being layered one on top of another in the stated order on the substrate **9011**. The organic semiconductor layers **9017***a*, **9017***b* are formed by applying organic semiconductor ink onto the insulating layer **9013** and by drying the applied organic semiconductor ink. The organic semiconductor layer **9017***a* is formed so as to fill the gap between the source electrode **9014***a* and the corresponding drain electrode and cover the source electrode **9014***a* and the corresponding drain electrode. Similarly, the organic semiconductor layer **9017***b* is formed so as to fill the gap between the source electrode **9014***b* and the corresponding drain electrode and cover the source electrode **9014***b* and the corresponding drain electrode.

[0005] In addition, as illustrated in FIG. **15**A, partition walls **9016** are formed on the insulating layer **9013**. The partition walls **9016** partition the organic semiconductor layer **9017***a* belonging to a first thin film transistor element from the organic semiconductor layer **9017***b* belonging to a second thin film transistor element that is adjacent to the first thin film transistor element. The partition walls **9016** define a plurality of apertures, namely apertures **9016***a* through **9016***c* in the case illustrated in FIG. **15**A. The aperture **9016***a* has a bottom portion where a connection wire **9015** that is connected with a drain electrode remains exposed. Further, an organic semiconductor layer is not formed with respect to the aperture **9016***a*. The connection wire **9015** is an electrode to be connected to an electrode of a light-emitting element portion to be formed above the organic TFT device. On the other hand, the organic semiconductor layers **9017***a*, **9017***b* are formed with respect to the apertures **9016***b*, **9016***c*, respectively. Note that the organic semiconductor layers **9017***a*, **9017***b* are partitioned from one another.

[0006] As already discussed above, a TFT device such as the organic TFT device illustrated in FIG. **15**A is used in a liquid crystal display panel, an organic EL display panel, or the like. Further, such a TFT device controls light emission of a light-emitting element portion according to signals input to the gate electrodes **9012***a*, **9012***b*, for instance, in the case illustrated in FIG. **15**A.

CITATION LIST

Patent Literature

[Patent Literature 1]

[0007] Japanese Patent Application Publication No. 2009-76791

SUMMARY

[0008] One problem in a conventional TFT device such as the one described above is the formation of an organic semiconductor layer with respect to an area of the TFT device where the formation of an organic semiconductor layer is undesirable (e.g., an inside of the aperture **9016***a* in the case illustrated in FIG. **15**A). The formation of an organic semiconductor layer at such an area of the TFT device results in poor electrical connection between the TFT device and other elements (for instance, the above-described light-emitting element portion), and hence, is problematic. In specific, as illustrated in FIG. **15**B, when respectively applying (dropping) organic semiconductor ink **90170***a*, **90170***b* with respect to the apertures **9016***b*, **9016***c* defined by the partition walls **9016**, there are cases where the organic semiconductor ink **90170***a*, **90170***b* overflows, flows out from the apertures **9016***b*, **9016***c*, and flows into the aperture **9016***a* (as indicated by arrow F_{91} in FIG. **15**B). This results in the connection wire **9015**, which is provided for electrical connection, being covered by an organic semiconductor layer.

[0009] It can be assumed that the above-described problem is likely to occur especially in a liquid crystal display panel, an organic EL display panel, etc. This is since there is a demand for realizing a liquid crystal display panel, an organic EL display panel, etc., with higher definition, which gives rise to a demand for downsizing subpixels therein. When the downsizing of subpixels is performed in response to such a demand, the distances between the above-described apertures are shortened, and the risk increases of ink overflowing from a given aperture and flowing into another aperture. As such, the above-described problem is likely to take place.

[0010] In addition, as illustrated in FIG. **15**B, the application of the organic semiconductor ink **90170***a*, **90170***b* with respect to the inside of the apertures **9016***b*, **9016***c* is performed such that the organic semiconductor ink **90170***a*, **90170***b* after application bulge upwards such that a top surface of the organic semiconductor ink **90170***a*, **90170***b* after application is higher in level than top surfaces of the partition walls **9016**. Due to this, there may be cases where the organic semiconductor ink **90170***a* and the organic semiconductor ink **90170***b* meet and blend with each other (as indicated by arrow F_{92} in FIG. **15**B). This results in the organic semicon-

ductor layers **9017***a*, **9017***b* being provided with undesirable layer-thicknesses. Further, when it is desired to form each of the organic semiconductor layers **9017***a*, **9017***b* as an organic semiconductor layer containing different components from the other, the above-described meeting and blending of organic semiconductor ink results in degradation of transistor performance.

[0011] It can be assumed that the above-described problem is likely to occur especially in a liquid crystal display panel, an organic EL display panel, etc. This is since, as already described above, there is a demand for realizing a liquid crystal display panel, an organic EL display panel, etc., with higher definition, which gives rise to a demand for downsizing subpixels therein. When the downsizing of subpixels is performed in response to such a demand, the distance between the aperture **9016***b* and the aperture **9016***c* is shortened, and the risk increases of the organic semiconductor ink **90170***a* and the organic semiconductor ink **90170***b* meeting and blending with each other.

[0012] Note that the same problems as described above can be expected to occur when an inorganic semiconductor layer is to be formed according to the application method, instead of an organic semiconductor layer.

[0013] Non-limiting and exemplary embodiments provide a thin film transistor device having high quality and a manufacturing method thereof, an organic EL display element, and an organic EL display device. Such a high-quality thin film transistor device is realized by, upon formation of a semiconductor layer of the thin film transistor device, preventing formation of a semiconductor layer at an area where the formation of an organic semiconductor layer is undesirable and preventing the meeting and blending of ink applied with respect to adjacent apertures.

[0014] In one general aspect, the techniques disclosed here feature a thin film transistor device having the following structure.

[0015] The thin film transistor device comprises: a first thin-film transistor element and a second thin-film transistor element that are arranged so as to be adjacent to each other with a gap therebetween, wherein each of the first thin-film transistor element and the second thin-film transistor element comprises: a gate electrode; an insulating layer disposed on the gate electrode; a source electrode and a drain electrode disposed on the insulating layer, the source electrode and the drain electrode being disposed with a gap therebetween; a semiconductor layer disposed on the source electrode and the drain electrode so as to cover the source electrode and the drain electrode and fill the gap between the source electrode and the drain electrode, and being in contact with the source electrode and the drain electrode; and a liquid-philic layer disposed on the insulating layer and having higher liquid philicity than the insulating layer, the liquid-philic layer being separate from the source electrode and the drain electrode.

[0016] In the thin film transistor device, the thin-film transistor device further comprises partition walls disposed on the insulating layer and partitioning the semiconductor layer of the first thin-film transistor element from the semiconductor layer of the second thin-film transistor element, the partition walls having liquid-repellant surfaces and defining a first aperture, a second aperture, and a third aperture, the first aperture surrounds at least a part of each of the source electrode, the drain electrode, and the liquid-philic layer of the first thin film transistor element, the second aperture is adjacent to the first aperture and surrounds at least a part of each of the source electrode, the drain electrode, and the liquid-philic layer of the second thin film transistor element, the third aperture is adjacent to the first aperture with a gap therebetween and is located in a direction, from the first aperture, differing from a direction of the second aperture.

[0017] In the thin film transistor device, an area of the thin-film transistor device surrounded by the third aperture does not include a semiconductor layer and does not function as a channel portion of the thin-film transistor device.

[0018] In the thin film transistor device, a bottom portion of each of the first and second apertures includes a source electrode portion being a bottom portion of the source electrode, a drain electrode portion being a bottom portion of the drain electrode, and a liquid-philic layer portion being a bottom portion of the liquid-philic layer, in plan view, at the bottom portion of the first aperture, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the third aperture, and in plan view, at the bottom portion of one of the first and second apertures, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the other one of the first and second apertures.

[0019] According to the above-described structure of the thin film transistor device, the bottom portion of the first aperture includes the liquid-philic layer portion, and at the bottom portion of the first aperture, the center of area of the liquid-philic layer portion is offset from the center of area of the bottom portion in a direction differing from the direction of the third aperture. Due to this, when semiconductor ink for forming the semiconductor layer is applied with respect to the first aperture during the manufacture of the thin film transistor device, a surface of the semiconductor ink applied with respect to the first aperture exhibits a shape such that the height of the surface of the applied semiconductor ink at a side of the first aperture in a direction differing from the direction of the third aperture is greater than the height of the surface of the applied semiconductor ink at a side of the first aperture in the direction of the third aperture. In other words, when the semiconductor ink is applied (i.e., when drops of the semiconductor ink are dropped) with respect to the first aperture, the surface of the applied semiconductor ink at a side of the first aperture in the direction of the third aperture can be configured to be lower in height compared to the surface of the applied semiconductor ink at a side of the first aperture at which the liquid-philic layer portion is located.

[0020] As such, according to the above-described structure, in the manufacture of the thin film transistor device, semiconductor ink is prevented from overflowing and flowing out towards the third aperture, and thus, formation of a semiconductor layer at an area of the thin film transistor device that does not function as a channel portion is prevented. Further, by preventing semiconductor ink from overflowing and flowing out as described above, a layer thickness of the semiconductor layer formed within the first aperture can be controlled with high accuracy.

[0021] In addition, according to the above-described structure, in plan view, at the bottom portion of one of the first and second apertures, the center of area of the liquid-philic layer portion is offset from the center of area of the bottom portion in a direction differing from the direction of the other one of the first and second apertures. Due to this, when semiconductor ink for forming the semiconductor layer is applied (i.e.,

when drops of the semiconductor ink are dropped) with respect to the first and second apertures during the manufacture of the thin film transistor device, the surface of the semiconductor ink applied with respect to the one of the first and second apertures exhibits a shape such that the height of the surface of the applied semiconductor ink at a side of the one of the first and second apertures in a direction differing from the direction of the other one of the first and second apertures is greater than the height of the surface of the applied semiconductor ink at a side of the one of the first and second apertures in the direction of the other one of the first and second apertures.

[0022] As such, according to the above-described structure, in the manufacture of the thin film transistor device, semiconductor ink applied with respect to one of the first and second apertures is prevented from undesirably meeting and blending with semiconductor ink applied with respect to the other one of the first and second apertures. Therefore, the first and the second thin film transistor elements can be formed with high accuracy, particularly in terms of the material composing the respective semiconductor layers and the layer thickness of the respective semiconductor layers.

[0023] As such, the thin film transistor device has a high quality that is realized by, upon formation of the semiconductor layer of the thin film transistor device, preventing formation of a semiconductor layer at an area where the formation of an organic semiconductor layer is undesirable and preventing the meeting and blending of ink applied with respect to adjacent apertures.

[0024] These general and specific aspects may be implemented by using an organic EL display element, an organic EL display device, and a method of manufacturing a thin film transistor device.

[0025] Additional benefits and advantages of the disclosed embodiments will be apparent from the specification and figures. The benefits and/or advantages may be individually provided by the various embodiments and features of the specification and drawings disclosed, and need not all be provided in order to obtain one or more of the same.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. **1** is a schematic block diagram illustrating an overall structure of an organic EL display device **1** pertaining to embodiment 1 of the present disclosure.

[0027] FIG. **2** is a schematic cross-sectional view illustrating a partial structure of an organic EL display panel **10**.

[0028] FIG. **3** is a schematic plan view illustrating a partial structure of a TFT substrate **101**.

[0029] FIG. **4**A is a process flow diagram providing an overview of a method of manufacturing the organic EL display panel **10**, and FIG. **4**B is a process flow diagram providing an overview of a method of forming the TFT substrate **101**.

[0030] FIGS. **5**A through **5**C are schematic process diagrams illustrating some procedures among procedures involved in the manufacturing of the TFT substrate **101**.

[0031] FIGS. **6**A through **6**C are schematic process diagrams illustrating some procedures among procedures involved in the manufacturing of the TFT substrate **101**.

[0032] FIG. **7**A is a schematic plan view illustrating a procedure among procedures involved in the manufacturing of the TFT substrate **101**, FIG. **7**B is a schematic cross-sectional view illustrating a structure along a cross section A-A' in FIG. **7**A, and FIG. **7**C is a schematic cross-sectional view illustrating a structure along a cross section B-B' in FIG. **7**A.

[0033] FIGS. **8**A and **8**B are schematic process diagrams illustrating some procedures among procedures involved in the manufacturing of the TFT substrate **101**.

[0034] FIG. **9**A is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 2, a partial structure of a TFT substrate, FIG. **9**B is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 3, a partial structure of a TFT substrate, and FIG. **9**C is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 4, a partial structure of a TFT substrate.

[0035] FIG. **10**A is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 5, a partial structure of a TFT substrate, FIG. **10**B is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 6, a partial structure of a TFT substrate, and FIG. **10**C is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 7, a partial structure of a TFT substrate.

[0036] FIG. **11**A is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 11, a partial structure of a TFT substrate, FIG. **11**B is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 12, a partial structure of a TFT substrate, and FIG. **11**C is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 13, a partial structure of a TFT substrate.

[0037] FIG. **12**A is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 14, a partial structure of a TFT substrate, and FIG. **12**B is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 15, a partial structure of a TFT substrate.

[0038] FIG. **13** is a schematic plan view illustrating, in a structure of an organic EL display panel pertaining to embodiment 16, a partial structure of a TFT substrate.

[0039] FIG. **14**A is a schematic plan view illustrating a shape of an opening of an aperture defined by partition walls in a TFT substrate pertaining to modification 1, FIG. **14**B is a schematic plan view illustrating a shape of an opening of an aperture defined by partitions wall in a TFT substrate pertaining to modification 2, and FIG. **14**C is a schematic plan view illustrating a shape of an opening of an aperture defined by partition walls in a TFT substrate pertaining to modification 3.

[0040] FIG. **15**A is a cross-sectional view illustrating, in a structure of an organic EL display device pertaining to conventional technology, a partial structure of a TFT substrate, and FIG. **15**B is a cross-sectional view illustrating a procedure pertaining to application of organic semiconductor ink among procedures involved in the manufacturing of the TFT substrate pertaining to conventional technology.

DETAILED DESCRIPTION

Overview of Aspects of Present Invention

[0041] One aspect of the present invention is a first thin-film transistor element and a second thin-film transistor element that are arranged so as to be adjacent to each other with

a gap therebetween, wherein each of the first thin-film transistor element and the second thin-film transistor element comprises: a gate electrode; an insulating layer disposed on the gate electrode; a source electrode and a drain electrode disposed on the insulating layer, the source electrode and the drain electrode being disposed with a gap therebetween; a semiconductor layer disposed on the source electrode and the drain electrode so as to cover the source electrode and the drain electrode and fill the gap between the source electrode and the drain electrode, and being in contact with the source electrode and the drain electrode; and a liquid-philic layer disposed on the insulating layer and having higher liquid philicity than the insulating layer, the liquid-philic layer being separate from the source electrode and the drain electrode.

[0042] In the thin film transistor device pertaining to one aspect of the present invention, the thin-film transistor device further comprises partition walls disposed on the insulating layer and partitioning the semiconductor layer of the first thin-film transistor element from the semiconductor layer of the second thin-film transistor element, the partition walls having liquid-repellant surfaces and defining a first aperture, a second aperture, and a third aperture, the first aperture surrounds at least a part of each of the source electrode, the drain electrode, and the liquid-philic layer of the first thin film transistor element, the second aperture is adjacent to the first aperture and surrounds at least a part of each of the source electrode, the drain electrode, and the liquid-philic layer of the second thin film transistor element, the third aperture is adjacent to the first aperture with a gap therebetween and is located in a direction, from the first aperture, differing from a direction of the second aperture.

[0043] In the thin film transistor device pertaining to one aspect of the present invention, an area of the thin-film transistor device surrounded by the third aperture does not include a semiconductor layer and does not function as a channel portion of the thin-film transistor device.

[0044] In the thin film transistor device pertaining to one aspect of the present invention, a bottom portion of each of the first and second apertures includes a source electrode portion being a bottom portion of the source electrode, a drain electrode portion being a bottom portion of the drain electrode, and a liquid-philic layer portion being a bottom portion of the liquid-philic layer, in plan view, at the bottom portion of the first aperture, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the third aperture, and in plan view, at the bottom portion of one of the first and second apertures, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the other one of the first and second apertures.

[0045] In other words, at the bottom portion of the first aperture, the liquid-philic layer portion, which belongs to the liquid-philic layer having higher wettability than the insulating layer, is disposed so as to be offset in a direction differing from the direction of the third aperture. Further, at the bottom portion of one of the first and second apertures, the liquid-philic layer portion so as to be offset from the center of area of the bottom portion in a direction differing from the direction of the other one of the first and second apertures.

[0046] According to the above-described structure of the thin film transistor device pertaining to one aspect of the present invention, the bottom portion of the first aperture includes the liquid-philic layer portion, and at the bottom portion of the first aperture, the center of area of the liquid-philic layer portion is offset from the center of area of the bottom portion in a direction differing from the direction of the third aperture. Due to this, when semiconductor ink for forming the semiconductor layer is applied with respect to the first aperture during the manufacture of the thin film transistor device, a surface of the semiconductor ink applied with respect to the first aperture exhibits a shape such that the height of the surface of the applied semiconductor ink at a side of the first aperture in a direction differing from the direction of the third aperture is greater than the height of the surface of the applied semiconductor ink at a side of the first aperture in the direction of the third aperture. In other words, when the semiconductor ink is applied (i.e., when drops of the semiconductor ink are dropped) with respect to the first aperture, the surface of the applied semiconductor ink at a side of the first aperture in the direction of the third aperture can be configured to be lower in height compared to the surface of the applied semiconductor ink at a side of the first aperture at which the liquid-philic layer portion is located.

[0047] As such, according to the above-described structure of the thin film transistor device pertaining to one aspect of the present invention, in the manufacture of the thin film transistor device, semiconductor ink is prevented from overflowing and flowing out towards the third aperture, and thus, formation of a semiconductor layer at an area of the thin film transistor device that does not function as a channel portion is prevented. Further, by preventing semiconductor ink from overflowing and flowing out as described above, a layer thickness of the semiconductor layer formed within the first aperture can be controlled with high accuracy.

[0048] In addition, according to the above-described structure of the thin film transistor device pertaining to one aspect of the present invention, in plan view, at the bottom portion of one of the first and second apertures, the center of area of the liquid-philic layer portion is offset from the center of area of the bottom portion in a direction differing from the direction of the other one of the first and second apertures. Due to this, when semiconductor ink for forming the semiconductor layer is applied (i.e., when drops of the semiconductor ink are dropped) with respect to the first and second apertures during the manufacture of the thin film transistor device, the surface of the semiconductor ink applied with respect to the one of the first and second apertures exhibits a shape such that the height of the surface of the applied semiconductor ink at a side of the one of the first and second apertures in a direction differing from the direction of the other one of the first and second apertures is greater than the height of the surface of the applied semiconductor ink at a side of the one of the first and second apertures in the direction of the other one of the first and second apertures.

[0049] As such, according to the above-described structure of the thin film transistor device pertaining to one aspect of the present invention, in the manufacture of the thin film transistor device, semiconductor ink applied with respect to one of the first and second apertures is prevented from undesirably meeting and blending with semiconductor ink applied with respect to the other one of the first and second apertures. Therefore, the first and the second thin film transistor elements can be formed with high accuracy, particularly in terms of the material composing the respective semiconductor layers and the layer thickness of the respective semiconductor layers.

[0050] As such, the thin film transistor device pertaining to one aspect of the present invention has a high quality that is realized by, upon formation of the semiconductor layer of the thin film transistor device, preventing formation of a semiconductor layer at an area where the formation of an organic semiconductor layer is undesirable and preventing the meeting and blending of ink applied with respect to adjacent apertures.

[0051] In the thin film transistor device pertaining to one aspect of the present invention, the bottom portion of the first aperture may include a first portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer of the first thin film transistor element is in direct contact with the semiconductor layer of the first thin film transistor element, the first portion being within an area of the bottom portion located in the direction of the third aperture. According to this, when semiconductor ink for forming the semiconductor layer is applied (i.e., when drops of the semiconductor ink are dropped) with respect to the first aperture during the manufacture of the thin film transistor device, a surface of the semiconductor ink applied with respect to the first aperture exhibits a shape such that the height of the surface of the applied semiconductor ink at a side of the first aperture in a direction differing from the direction of the third aperture is greater than the height of the surface of the applied semiconductor ink at a side of the first aperture in the direction of the third aperture with higher certainty. As such, semiconductor ink is prevented from overflowing and flowing into the third aperture with certainty, and hence, a thin film semiconductor device having high quality is realized.

[0052] In the thin film transistor device pertaining to one aspect of the present invention, the bottom portion of the first aperture may further include a second portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer of the first thin film transistor element is in direct contact with the semiconductor layer of the first thin film transistor element, the second portion being within an area of the bottom portion located in a direction differing from the direction of the third aperture, and in plan view of the bottom portion of the first aperture, an area of the first portion may be greater than an area of the second portion. According to this structure, the surface of the ink applied with respect to the first aperture exhibits, to a further extent, the shape as described above. As such, semiconductor ink is prevented from overflowing and flowing into the third aperture with certainty.

[0053] In the thin film transistor device pertaining to one aspect of the present invention, in plan view, at the bottom portion of the other one of the first and second apertures, a center of area of the liquid-philic layer portion may be offset from a center of area of the bottom portion in a direction differing from a direction of the one of the first and second apertures. According to this structure, when semiconductor ink is applied with respect to both the first and second apertures during the manufacture of the thin film transistor device, the meeting and blending of semiconductor ink applied with respect to the first aperture and semiconductor ink applied with respect to the second aperture is prevented with higher certainty.

[0054] In the thin film transistor device pertaining to one aspect of the present invention, in plan view of the first, second, and third apertures, the third aperture, the first aperture, and the second aperture may be arranged in series in the stated order along a predetermined direction, at the bottom portion of the first aperture, the center of area of the liquid-philic layer portion may be offset from the center of area of the bottom portion in a first direction that intersects the predetermined direction, and at the bottom portion of the second aperture, the center of area of the liquid-philic layer portion may be offset from the center of area of the bottom portion in a second direction that intersects the predetermined direction. By disposing the liquid-philic layer portions in the first and second apertures according to this structure, when semiconductor ink is applied with respect to both the first and second apertures during the manufacture of the thin film transistor device, semiconductor ink can be prevented from overflowing and flowing into the third aperture, and at the same time, the meeting and blending of semiconductor ink applied with respect to the first aperture and semiconductor ink applied with respect to the second aperture can be prevented.

[0055] In the thin film transistor device pertaining to one aspect of the present invention, the first direction and the second direction may be opposite directions. According to this structure, the undesirable meeting and blending of semiconductor ink applied with respect to the first aperture and semiconductor ink applied with respect to the second aperture can be prevented with higher certainty.

[0056] In the thin film transistor device pertaining to one aspect of the present invention, in each of the first and second thin film transistor elements, the liquid-philic layer may be formed by using a same material as used for forming the source electrode and the drain electrode, and the liquid-philic layer may be located apart from each of the source electrode and the drain electrode. According to this structure, the forming of the liquid-philic layers can be performed in the same manufacturing procedure as the forming of the source electrodes and the drain electrodes, and hence, an increase in procedures during the manufacture of the thin film transistor device is not brought about. As such, an advantageous effect is achieved in that a reduction in manufacturing cost is realized.

[0057] Note that, by forming the liquid-philic layer so as to be located apart from each of the source electrode and the drain electrode, the risk is eliminated of transistor performance being affected when forming the liquid-philic layer by using the same material as used for forming the source electrode and the drain electrode.

[0058] In the thin film transistor device pertaining to one aspect of the present invention, in plan view of the bottom portions of the first and second apertures, at the bottom portion of each of the first and second apertures, a center of area of each of the source electrode portion and the drain electrode portion may coincide with the center of area of the bottom portion. According to this structure, by disposing the source electrode and the drain electrode such that, at the bottom portion of each of the first and second apertures, the center of a total of areas of the source electrode portion and the drain electrode portion coincides with the center of area of the bottom portion, high transistor performance can be maintained. In addition, by disposing the liquid-philic layer portion so as to be in an offset arrangement as described above, semiconductor ink can be prevented from flowing out towards the third aperture with certainty and the meeting and blending of semiconductor ink applied with respect to the respective apertures can be prevented with certainty.

[0059] In the thin film transistor device pertaining to one aspect of the present invention, in plan view of the bottom

portions of the first and second apertures, at the bottom portion of the first aperture, a center of a total of areas of the source electrode portion, the drain electrode portion, and the liquid-philic layer portion may be offset from the center of area of the bottom portion in a direction differing from the direction of the third aperture, and at the bottom portion of the second aperture, a center of a total of areas of the source electrode portion, the drain electrode portion, and the liquid-philic layer portion may be offset from the center of area of the bottom portion in a direction differing from the direction of the first aperture. According to this structure, when semiconductor ink is applied with respect to each of the first and second apertures during the manufacture of the thin film transistor device, the surface of the semiconductor ink applied with respect to the first aperture is biased in a direction differing from the direction of the third aperture, and the shape of the surface of the semiconductor ink applied with respect to the first aperture and the shape of the surface of the semiconductor ink applied with respect to the second aperture differ from each other for being biased in different directions. This is due to the relationship between the liquid repellency of the insulating layer and the liquid repellency of the liquid-philic layer, the source electrode, and the drain electrode. As such, semiconductor ink applied with respect to the first aperture is prevented from flowing out towards the inside of the third aperture, and further, the meeting and blending of semiconductor ink applied with respect to the first aperture and the semiconductor ink applied with respect to the second aperture can be prevented.

[0060] Note that, when denoting: the area of the source electrode portion as A_S; a distance from a given point to the center of area of the source electrode portion as X_S; the area of the drain electrode portion as A_D; a distance from the given point to the center of area of the drain electrode portion as X_D, the area of the liquid-philic layer portion as A_H; and a distance from the given point to the center of area of the liquid-philic layer portion as X_H, "a center of a total of areas of the source electrode portion, the drain electrode portion, and the liquid-philic layer portion", denoted as z, can be expressed as shown in Math. 1.

$$z=(A_S\times x_S+A_D\times x_D\times A_H\times x_H)/(A_S+A_D+A_H) \quad \text{[Math. 1]}$$

[0061] In the thin film transistor device pertaining to one aspect of the present invention, at the bottom portion of the first aperture, a side of the liquid-philic layer portion located in the direction of the third aperture may be located apart from a side surface portion, of the partition walls, facing the first aperture, and a side of the liquid-philic layer portion located in a direction differing from the direction of the third aperture may be in contact with the side surface portion, of the partition walls, facing the first aperture.

[0062] The above-described effects can also be achieved by disposing the liquid-philic layer portion in the first aperture according to this structure.

[0063] In the thin film transistor device pertaining to one aspect of the present invention, a liquid repellency of the surfaces of the partition walls may be greater than a liquid repellency of a surface of the insulating layer, in each of the first and second thin film transistor elements, that is in contact with the semiconductor layer, and the liquid repellency of the surface of the insulating layer, in each of the first and second thin film transistor elements, that is in contact with the semiconductor layer may be greater than a liquid repellency of a surface of each of the source electrode, the drain electrode, and the liquid-philic layer in each of the first and second thin film transistor elements. When the above-described relationship is satisfied, the surface of the semiconductor ink applied with respect to the first aperture and the surface of the semiconductor ink applied with respect to the second aperture exhibit the respective shapes as described above when the application of semiconductor ink is performed in the manufacture of the thin film transistor device, and hence, the above-described effects can be achieved with certainty.

[0064] In the thin film transistor device pertaining to one aspect of the present invention, a bottom portion of the third aperture may includes a wire for electrically connecting with one of the source electrode and the drain electrode in the first thin film transistor element or one of the source electrode and the drain electrode in the second thin film transistor element. When the third aperture is used as a contact area in the thin film transistor device for outputting signals from the thin film transistor elements to the outside, the formation of a semiconductor layer with respect to the connection wire is to be prevented. Here, by employing the above-described structure, the flowing out of semiconductor ink towards the third aperture upon application of semiconductor ink is prevented with certainty, and thus, it is ensured that the third aperture maintains the function as the contact area.

[0065] One aspect of the present invention is an organic EL display element comprising: any of the thin film transistor devices described above; a planarizing film formed above the thin film transistor device and having a contact hole formed therein; a lower electrode formed on the planarizing film so as to cover the planarizing film and a side surface of the planarizing film defining the contact hole, and electrically connected with one of the source electrode and the drain electrode in the first thin film transistor element or one of the source electrode and the drain electrode in the second thin film transistor element; an upper electrode formed above the lower electrode; and an organic light-emitting layer interposed between the lower electrode and the upper electrode, wherein the contact hole is in communication with the third aperture of the thin film transistor device.

[0066] According to this, since the organic EL display element pertaining to one aspect of the present invention includes any of the thin film transistor devices described above, the organic EL element is ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0067] One aspect of the present invention is an organic EL display device comprising the organic EL display element described above. According to this, the organic EL display device is also ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0068] One aspect of the present invention is a method of manufacturing a thin film transistor device comprising:

[0069] forming a first gate electrode and a second gate electrode on a substrate so as to be adjacent to each other with a gap therebetween;

[0070] forming an insulating layer so as to cover the first gate electrode and the second gate electrode;

[0071] forming first and second source electrodes, first and second drain electrodes, and first and second liquid-philic layers on the insulating layer, wherein (i) the first source electrode and the first drain electrode are formed with respect to the first gate electrode with a gap therebetween, (ii) the second source electrode and the second drain electrode are formed with respect to the sec-

ond gate electrode with a gap therebetween, (iii) the first liquid-philic layer is formed with respect to the first source electrode and the first drain electrode so as to be located apart from the first source electrode and the first drain electrode, the first liquid-philic layer having higher liquid philicity than the insulating layer, and (iv) the second liquid-philic layer is formed with respect to the second source electrode and the second drain electrode so as to be located apart from the second source electrode and the second drain electrode, the second liquid-philic layer having higher liquid philicity than the insulating layer;

[0072] depositing a layer of photosensitive resist material such that, above the insulating layer, the layer of photosensitive resist material covers the first and second source electrodes and the first and second drain electrodes as well as areas therearound;

[0073] forming partition walls on the insulating layer by performing mask exposure and patterning of the layer of photosensitive resist material, the partition walls having liquid-repellant surfaces and defining a first aperture, a second aperture that is adjacent to the first aperture, and a third aperture, the first aperture surrounding at least a part of each of the first source electrode, the first drain electrode, and the first liquid-philic layer, the second aperture surrounding at least a part of each of the second source electrode, the second drain electrode, and the second liquid-philic layer; and

[0074] forming a first semiconductor layer with respect to the first aperture and a second semiconductor layer with respect to the second aperture by applying semiconductor material with respect to the corresponding aperture and drying the semiconductor material so applied, wherein (i) the first semiconductor layer is formed so as to be in contact with the first source electrode and the first drain electrode, and (ii) the second semiconductor layer is formed so as to be in contact with the second source electrode and the second drain electrode.

[0075] In the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, the partition walls are formed such that the third aperture is adjacent to the first aperture with a gap therebetween and is located in a direction, from the first aperture, differing from a direction of the second aperture, a bottom portion of each of the first and second apertures includes a source electrode portion being a bottom portion of the corresponding source electrode, a drain electrode portion being a bottom portion of the corresponding drain electrode, and a liquid-philic layer portion being a bottom portion of the corresponding liquid-philic layer, in plan view, at the bottom portion of the first aperture, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the third aperture, and in plan view, at the bottom portion of one of the first and second apertures, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the other one of the first and second apertures.

[0076] According to the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, by disposing the liquid-philic layer portion with respect to the bottom portion of the first aperture as described above when forming the partition walls, when semiconductor ink for forming the semiconductor layer is applied with respect to the first aperture during the manufacture of the thin film transistor device, a surface of the semiconductor ink applied with respect to the first aperture exhibits a shape such that the height of the surface of the applied semiconductor ink at a side of the first aperture in a direction differing from the direction of the third aperture is greater than the height of the surface of the applied semiconductor ink at a side of the first aperture in the direction of the third aperture. In other words, when the semiconductor ink is applied (i.e., when drops of the semiconductor ink are dropped) with respect to the first aperture, the surface of the applied semiconductor ink at a side of the first aperture in the direction of the third aperture can be configured to be lower in height compared to the surface of the applied semiconductor ink at a side of the first aperture at which the liquid-philic layer portion is located in an offset manner.

[0077] As such, according to the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, semiconductor ink is prevented from overflowing and flowing out towards the third aperture, and thus, formation of a semiconductor layer at an area of the thin film transistor device that does not function as a channel portion is prevented. Further, by preventing semiconductor ink from overflowing and flowing out as described above, a layer thickness of the semiconductor layer formed within the first aperture can be controlled with high accuracy.

[0078] In addition, according to the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, the formation of the partition walls is performed such that, at the bottom portion of one of the first and second apertures, the center of area of the liquid-philic layer portion is offset from the center of area of the bottom portion in a direction differing from the direction of the other one of the first and second apertures. Due to this, when semiconductor ink for forming the semiconductor layer is applied (i.e., when drops of the semiconductor ink are dropped) with respect to the first and second apertures during the manufacture of the thin film transistor device, the surface of the semiconductor ink applied with respect to the one of the first and second apertures exhibits a shape such that the height of the surface of the applied semiconductor ink at a side of the one of the first and second apertures in a direction differing from the direction of the other one of the first and second apertures is greater than the height of the surface of the applied semiconductor ink at a side of the one of the first and second apertures in the direction of the other one of the first and second apertures.

[0079] As such, according to the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, in the manufacture of the thin film transistor device, semiconductor ink applied with respect to one of the first and second apertures is prevented from undesirably meeting and blending with semiconductor ink applied with respect to the other one of the first and second apertures. Therefore, the first and the second thin film transistor elements can be formed with high accuracy, particularly in terms of the material composing the respective semiconductor layers and the layer thickness of the respective semiconductor layers.

[0080] As such, according to the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, a thin film transistor device having a high quality can be manufactured by, upon formation of the semi-

conductor layer of the thin film transistor device, preventing formation of a semiconductor layer at an area where the formation of an organic semiconductor layer is undesirable and preventing the meeting and blending of ink applied with respect to adjacent apertures.

[0081] In the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, the partition walls may be formed such that the bottom portion of the first aperture includes a first portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer is to come in direct contact with the first semiconductor layer, the first portion being within an area of the bottom portion located in the direction of the third aperture. According to this, the surface of the ink applied with respect to the first aperture exhibits, to a further extent, the shape as described above. As such, semiconductor ink is prevented from overflowing and flowing into the third aperture with certainty.

[0082] In the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, the partition walls may be formed such that the bottom portion of the first aperture further includes a second portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer is to come in direct contact with the first semiconductor layer, the second portion being within an area of the bottom portion located in a direction differing from the direction of the third aperture, and in plan view of the bottom portion of the first aperture, an area of the first portion may be greater than an area of the second portion. According to this, the surface of the ink applied with respect to the first aperture exhibits, to a further extent, the shape as described above. As such, semiconductor ink is prevented from overflowing and flowing into the third aperture with certainty.

[0083] In the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, the forming, on the insulating layer, of the first and second source electrodes, the first and second drain electrodes, and the first and second liquid-philic layers may include sub-steps of: forming a metal layer on the insulating layer; and etching the metal layer so formed. According to this, the forming of the first and second liquid-philic layers can be performed in the same manufacturing procedure as the forming of the first and second source electrodes and the first and second drain electrodes, and hence, an increase in procedures during the manufacture of the thin film transistor device is not brought about. As such, an advantageous effect is achieved in that a reduction in manufacturing cost is realized while the above-described affects are realized at the same time.

[0084] In the method of manufacturing a thin film transistor device pertaining to one aspect of the present invention, the forming of the insulating layer, the forming of the first and second source electrodes, the first and second drain electrodes, and the first and second liquid-philic layers, the forming of the partition walls, and the forming of the first and second semiconductor layers may be performed such that a liquid repellency of the surfaces of the partition walls is greater than a liquid repellency of a surface of the insulating layer that is to come in contact with the first and second semiconductor layers, and the liquid repellency of the surface of the insulating layer is greater than a liquid repellency of a surface of each of the first and second source electrodes, each of the first and second drain electrodes, and each of the first and second liquid-philic layers. When the above-described relationship is satisfied, the surface of the semiconductor ink applied with respect to the first aperture and the surface of the semiconductor ink applied with respect to the second aperture exhibit the respective shapes as described above when the application of semiconductor ink is performed in the manufacture of the thin film transistor device, and hence, the above-described effects can be achieved with certainty.

[0085] Note that in the above, when a given element is "on" or "above" another element, the given element is not limited to being disposed in the absolutely vertical direction with respect to the other element. Instead, in the present disclosure, the terms "on" and "above" are used to indicate the relative positions of different elements, or more specifically, the relative positions of different elements along the direction in which such elements are layered. Further, in the present disclosure, the term "above" is used to indicate not only a state where a gap exists between two elements, but also a state where the two elements are in close contact with each other, and similarly, the term "on" is used to indicate not only a state where two elements are in close contact with each other, but also a state where a gap exists between the two elements.

[0086] In the following, explanation is provided of characteristics of various forms of implementation and the effects achieved thereby, with reference to several specific examples thereof. Further, note that although the following embodiments include description on fundamental characteristic features, the present disclosure is not to be construed as being limited to the description provided in the following embodiments other than such fundamental features.

Embodiment 1

1. Overall Structure of Organic EL Display Device **1**

[0087] In the following, description is provided on a structure of an organic EL display device **1** pertaining to embodiment 1 of the present disclosure, with reference to FIG. **1**.

[0088] As illustrated in FIG. **1**, the organic EL display device **1** includes an organic EL display panel **10** and a drive control circuit portion **20** connected to the organic EL display panel **10**.

[0089] The organic EL display panel **10** is a panel that makes use of electroluminescence of organic material. The organic EL display panel **10** is composed of a plurality of organic EL elements that are, for instance, arranged so as to form a matrix. The drive control circuit portion **20** includes four drive circuits, namely drive circuits **21** through **24**, and a control circuit **25**.

[0090] Note that, in the organic EL display device **1** pertaining to the present embodiment, the positional arrangement of the drive control circuit portion **20** with respect to the organic EL display panel **10** is not limited to that illustrated in FIG. **1**.

2. Structure of Organic EL Display Panel **10**

[0091] In the following, description is provided on a structure of the organic EL display panel **10**, with reference to the schematic cross-sectional view of FIG. **2** and the schematic plan view of FIG. **3**.

[0092] As illustrated in FIG. **2**, the organic EL display panel **10** includes a thin film transistor (TFT) substrate **101**. The TFT substrate **101** has a structure where gate electrodes **1012***a*, **1012***b* are layered on a substrate **1011** with a gap between one another, and an insulating layer **1013** is layered

so as to cover the substrate **1011** and the gate electrodes **1012***a*, **1012***b*. On the insulating layer **1013**, a source electrode **1014***a* and a drain electrode **1014***c* corresponding to the gate electrode **1012***a* are disposed, and similarly, a source electrode **1014***b* and a drain electrode **1014***d* corresponding to the gate electrode **1012***b* are disposed. As illustrated in FIG. **3**, the source electrode **1014***a* and the drain electrode **1014***c* are arranged on the insulating layer **1013** so as to be in alignment in the X axis direction in FIG. **3**, and similarly, the source electrode **1014***b* and the drain electrode **1014***d* are arranged so as to be in alignment in the X axis direction in FIG. **3**.

[0093] In addition, as illustrated in FIG. **2** and FIG. **3**, a connection wire **1015** is disposed on the insulating layer **1013** at the left side of the source electrode **1014***a* in the X axis direction, and such that there is a gap between the connection wire **1015** and the source electrode **1014***a*. The connection wire **1015** is formed by extending one of the source electrode **1014***a*, the drain electrode **1014***c*, the source electrode **1014***b*, and the drain electrode **1014***d*. Alternatively, the connection wire **1015** is electrically connected to one of the source electrode **1014***a*, the drain electrode **1014***c*, the source electrode **1014***b*, and the drain electrode **1014***d*.

[0094] Further, as illustrated in FIG. **3**, a liquid-philic layer **1019***a* is disposed on the insulating layer **1013**. The liquid-philic layer **1019***a* is disposed upwards in the Y axis direction with respect to the source electrode **1014***a* and the drain electrode **1014***c*, and so as to be apart from the source electrode **1014***a* and the drain electrode **1014***c*. Similarly, a liquid-philic layer **1019***b* corresponding to the combination of the source electrode **1014***b* and the drain electrode **1014***d* is disposed on the insulating layer **1013**. The liquid-philic layer **1019***b* is disposed downwards in the Y axis direction with respect to the source electrode **1014***b* and the drain electrode **1014***d*, and so as to be apart from the source electrode **1014***b* and the drain electrode **1014***d*. In the present embodiment, the liquid-philic layers **1019***a*, **1019***b* are formed by using the same material as used for forming the source electrodes **1014***a*, **1014***b* and the drain electrodes **1014***c*, **1014***d*.

[0095] Further, as illustrated in FIGS. **2** and **3**, partition walls **1016** are disposed on the insulating layer **1013**. The partition walls **1016** surround (a) the connection wire **1015**, (b) a combination of the source electrode **1014***a*, the drain electrode **1014***c*, and the liquid-philic layer **1019***a*, and (c) a combination of the source electrode **1014***b*, the drain electrode **1014***d*, and the liquid-philic layer **1019***b*, in such a manner that (a), (b), and (c) are separated from one another by being surrounded by the partition walls **1016**. In other words, as illustrated in FIG. **3**, the partition walls **1016** define three apertures, namely an aperture **1016***a*, an aperture **1016***b*, and an aperture **1016***c*. The aperture **1016***a* at the far left side in the X axis direction has a bottom portion where the connection wire **1015** remains exposed. The aperture **1016***a* does not function as a channel portion but functions as a contact portion that contacts an anode. On the other hand, the aperture **1016***b* has a bottom portion where the source electrode **1014***a*, the drain electrode **1014***c*, and the liquid-philic layer **1019***a* remain exposed, and the aperture **1016***c* has a bottom portion where the source electrode **1014***b*, the drain electrode **1014***d*, and the liquid-philic layer **1019***b* remain exposed. The apertures **1016***b* and **1016***c* function as channel portions.

[0096] At the bottom portion of the aperture **1016***b*, a left side of the source electrode **1014***a* in the X axis direction is in contact with a side surface portion, of the partition walls **1016**, facing the aperture **1016***b*, and a right side of the drain electrode **1014***c* in the X axis direction is in contact with the side surface portion facing the aperture **1016***b*. The three remaining sides of the source electrode **1014***a* are located apart from the side surface portion facing the aperture **1016***b*, and similarly, the three remaining sides of the drain electrode **1014***c* are located apart from the side surface portion facing the aperture **1016***b*. Further, the liquid-philic layer **1019***a* is in contact with the side surface portion facing the aperture **1016***b* at three sides thereof, namely both sides thereof in the X axis direction and an upper side thereof in the Y axis direction.

[0097] At the bottom portion of the aperture **1016***c*, a left side of the source electrode **1014***b* in the X axis direction is in contact with a side surface portion, of the partition walls **1016**, facing the aperture **1016***c*, and a right side of the drain electrode **1014***d* in the X axis direction is in contact with the side surface portion facing the aperture **1016***c*. The three remaining sides of the source electrode **1014***b* are located apart from the side surface portion facing the aperture **1016***c*, and similarly, the three remaining sides of the drain electrode **1014***d* are located apart from the side surface portion facing the aperture **1016***c*. Further, the liquid-philic layer **1019***b* is in contact with the side surface portion facing the aperture **1016***c* at three sides thereof, namely both sides thereof in the X axis direction and a lower side thereof in the Y axis direction.

[0098] In addition, as illustrated in FIG. **3**, at the bottom portion of the aperture **1016***b*, a portion of the insulating layer **1013** remains exposed at a lower side of the bottom portion in the Y axis direction (such portion hereinafter referred to as an exposed portion **1013***a*). Similarly, as illustrated in FIG. **3**, at the bottom portion of the aperture **1016***c*, a portion of the insulating layer **1013** remains exposed at an upper side of the bottom portion in the Y axis direction (such portion hereinafter referred to as an exposed portion **1013***b*).

[0099] Returning to FIG. **2**, within the aperture **1016***b* defined by the partition walls **1016**, an organic semiconductor layer **1017***a* is disposed on the source electrode **1014***a* and the drain electrode **1014***c* included therein. Similarly, within the aperture **1016***c* defined by the partition walls **1016**, an organic semiconductor layer **1017***b* is disposed on the source electrode **1014***b* and the drain electrode **1014***d*. More specifically, the organic semiconductor layer **1017***a* is formed so as to cover the source electrode **1014***a* and the drain electrode **1014***c* and also fill a gap between the source electrode **1014***a* and the drain electrode **1014**. The organic semiconductor layer **1017***a* so formed is in contact with the source electrode **1014***a* and the drain electrode **1014***c*. The organic semiconductor layer **1017***b* is formed in a similar manner and is in contact with the source electrode **1014***b* and the drain electrode **1014***d*. Further, the organic semiconductor layer **1017***a* and the organic semiconductor layer **1017***b* are partitioned from each other by the partition walls **1016**.

[0100] Here, note that within the aperture **1016***b*, the organic semiconductor layer **1017***a* is in direct contact with the insulating layer **1013** at the exposed portion **1013***a* illustrated in FIG. **3**, without the source electrode **1014***a* or the drain electrode **1014***c* existing therebetween. Similarly, within the aperture **1016***c*, the organic semiconductor layer **1017***b* is in direct contact with the insulating layer **1013** at the exposed portion **1013***b* illustrated in FIG. **3**, without the source electrode **1014***b* or the drain electrode **1014***d* existing therebetween. Also refer to FIG. **2** for illustration of the above.

[0101] Further, as illustrated in FIG. **2**, a passivation film **1018** is disposed so as to cover the organic semiconductor layer **1017***a*, the organic semiconductor layer **1017***b*, and the insulating layer **1013**. However, it should be noted that the passivation film **1018** is not disposed above the area surrounded by the aperture **1016***a*, which includes the connection wire **1015**.

[0102] The TFT substrate **101** of the organic EL display panel **10** pertaining to the present embodiment has a structure as described up to this point.

[0103] In the following, the entire structure of the organic EL display panel **10**, including the TFT substrate **101**, is explained. As illustrated in FIG. **2**, a planarizing film **102** covers the TFT substrate **101** from above. However, it should be noted that the planarizing film **102** does not cover the connection wire **1015**, and a contact hole **102***a* is formed in the planarizing film **102** at an area above the connection wire **1015**. The contact hole **102***a* is in communication with the aperture **1016***a* of the TFT substrate **101**.

[0104] An anode **103**, a light-transmissive conduction film **104**, and a hole injection layer **105** are disposed in the stated order on a main surface of the planarizing film **102**. Here, each of the anode **103**, the light-transmissive conduction film **104**, and the hole injection layer **105** is disposed not only on the planarizing film **102** but also along a side surface of the planarizing film **102** defining the contact hole **102***a*. The anode **103** is in contact with and electrically connected to the connection wire **1015**.

[0105] Further, banks **106** are disposed on the hole injection layer **105**. The banks **106** are disposed so as to surround an area above the hole injection layer **105** that corresponds to a light-emitting portion (i.e., a subpixel). In an opening formed at the above-described area by the banks **106**, a hole transport layer **107**, an organic light-emitting layer **108**, and an electron transport layer **109** are disposed in the stated order.

[0106] On the electron transport layer **109** and on exposed surfaces of the banks **106**, a cathode **110** and a sealing layer **111** are disposed in the stated order so as to cover the electron transport layer **109** and the exposed surfaces of the banks **106**. Further, a color filter (CF) substrate **113** is arranged so as to face the sealing layer **111**. The sealing layer **111** and the CF substrate **113** are joined together by an adhesion layer **112** filling a gap therebetween. The CF substrate **113** includes a substrate **1131**, and a color filter **1132** and a black matrix **1133** disposed on a main surface of the substrate **1131**. The main surface of the substrate **1131** is a surface of the substrate **1131** that is located lower in the Z axis direction.

3. Material Constituting Organic EL Display Panel **10**

[0107] Each part of the organic EL display panel **10** may, for instance, be formed by using the materials as described in the following.

[0108] (i) Substrate **1011**

[0109] The substrate **1011** may be, for instance: a glass substrate; a quartz substrate; a silicon substrate; a metal substrate composed of, for example, molybdenum sulfide, copper, zinc, aluminum, stainless steel, magnesium, iron, nickel, gold, or silver; a semiconductor substrate composed of, for example, gallium arsenide; or a plastic substrate.

[0110] Examples of material constituting the plastic substrate include thermoplastic resins and thermosetting resins. Examples thereof include polyolefins, such as polyethylene, polypropylene, ethylene-propylene copolymers, and ethylene-vinyl acetate copolymers (EVA), cyclic polyolefin, modified polyolefins, polyvinyl chloride, polyvinylidene chloride: polystyrene, polyamide, polyimide (PI), polyamide-imide, polyesters, such as polycarbonate, poly(4-methylpentene-1), ionomers, acrylic-based resins, polymethyl methacrylater acrylic-styrene copolymers (AS resins), butadiene-styrene copolymers, ethylene vinyl alcohol copolymers (EVOH), polyethylene terephthalate (PET), polybutylene terephthalate, polyethylene naphthalate (PEN), and polycyclohexane terephthalate (PCT), polyether, polyether ketone, polyethersulfone (PES), polyether imide, polyacetal, polyphenylene oxide, modified polyphenylene oxide, polyarylate, aromatic polyesters (liquid crystal polymer), polytetrafluoroethylene, polyvinylidene fluoride, other fluorocarbon resins, thermoplastic elastomers, such as styrene-based elastomers, polyolefin-based elastomers, polyvinyl chloride-based elastomers, polyurethane-based elastomers, fluorocarbon rubbers, and chlorinated polyethylene-based elastomers, epoxy resins, phenolic resins, urea resins, melamine resins, unsaturated polyesters, silicone resins, and polyurethane, and copolymers, blends, and polymer alloys thereof. The plastic substrate may be a single layer substrate composed of one of the materials described above or a multilayer substrate having layers composed of two or more materials.

[0111] (ii) Gate Electrodes **1012***a*, **1012***b*

[0112] The gate electrodes **1012***a*, **1012***b* may be made of, for instance, any material having electrical conductivity.

[0113] Specific examples thereof include metals, such as chromium, aluminum, tantalum, molybdenum, niobium, copper, silver, gold, platinum, palladium, indium, nickel, and neodymium, and alloys thereof; conductive metal oxides, such as zinc oxide, tin oxide, indium oxide, and gallium oxide; conductive metal complex oxides, such as indium tin complex oxide (ITO), indium zinc complex oxide (IZO), aluminum zinc complex oxide (AZO), and gallium zinc complex oxide (GZO); conductive polymers, such as polyaniline, polypyrrole, polythiophene, and polyacetylene, and conductive polymers doped with acids, e.g., hydrochloric acid, sulfuric acid, and sulfonic acid, Lewis acids, e.g., phosphorus pentafluoride, arsenic pentafluoride, and iron chloride, halogen elements, e.g., iodine, and metals, e.g., sodium and potassium; and conductive composite materials containing carbon black and metal particles dispersed. Alternatively, polymer mixtures containing conductive particles, such as fine metal particles and graphite, may be used. These materials may be used alone or in combination.

[0114] (iii) Insulating Layer **1013**

[0115] The insulating layer **1013** functions as a gate insulating layer. The insulating layer **1013** may be made, for instance, of any material having insulative properties. Examples of the material that can be used include organic insulating materials and inorganic insulating materials.

[0116] Examples of organic insulating materials include acrylic resins, phenolic resins, fluororesins, epoxy resins, imide resins, and novolac type resins.

[0117] Examples of inorganic insulating materials include: metal oxides, such as silicon oxide, aluminum oxide, tantalum oxide, zirconium oxide, cerium oxide, zinc oxide, and cobalt oxide; metal nitrides, such as silicon nitride, aluminum nitride, zirconium nitride, cerium nitride, zinc nitride, cobalt nitride, titanium nitride, and tantalum nitride; and metal complex oxides, such as barium strontium titanate and lead zirconate titanate. These may be used alone or in combination.

[0118] Further, the insulating layer **1013** may have a surface thereof processed by using a surface treatment agent (ODTS OTS HMDS βPTS) or the like.

[0119] (iv) Source Electrodes **1014***a*, **1014***b*, and Drain Electrodes **1014***c*, **1014***d*

[0120] The source electrodes **1014***a*, **1014***b* and the drain electrodes **1014***c*, **1014***d* can be formed by using the same materials as used for forming the gate electrodes **1012***a*, **1012***b*.

[0121] (v) Organic Semiconductor Layers **1017***a*, **1017***b*

[0122] The organic semiconductor layers **1017***a*, **1017***b* may be formed by using, for instance, any material that has semiconducting properties and is soluble to a solvent. Specific examples thereof include thiophene-based materials, such as poly(3-alkylthiophene), poly(3-hexylthiophene) (P3HT), poly(3-octylthiophene), poly(2,5-thienylene vinylene) (PTV), quarterthiophene (4T), sexithiophene (6T), octathiophene, 2,5-bis(5'-biphenyl-2'-thienyl)thiophene (BPT3), 2,5-[2,2'-(5,5'-diphenyl)dithienyl]thiophene, and [5,5'-bis(3-dodecyl-2-thienyl)-2,2'-bithiophene] (PQT-12); phenylene vinylene-based materials such as poly(paraphenylene vinylene) (PPV); fluorene-based materials such as poly(9,9-dioctylfluorene) (PFO); triallylamine-based polymers; acene-based materials, such as anthracene, tetracene, pentacene, and hexacene; benzene-based materials, such as 1,3,5-tris[(3-phenyl-6-trifluoromethyl)quinoxalin-2-yl]benzene (TPQ1) and 1,3,5-tris[{3-(4-tert-butylphenyl)-6-trisfluoromethyl}quinoxalin-2-yl]benzene (TPQ2); phthalocyanine-based materials, such as phthalocyanine, copper phthalocyanine (CuPc), iron phthalocyanine, and perfluorophthalocyanine; organometallic materials, such as tris(8-hydroxyquinoline) aluminum (Alq3) and fac-tris(2-phenylpyridine) iridium (Ir(ppy)3); C60; polymers, such as, oxadiazole-based polymers, triazole-based polymers, carbazole-based polymers, and fluorene-based polymers; poly(9,9-dioctylfluorene-co-bis-N,N'-(4-methoxyphenyl)-bis-N,N'-phenyl-1,4-phenylenediamine) (PFMO); poly(9,9-dioctylfluorene-co-benzothiadiazole) (BT); fluorene-triallylamine copolymers; and copolymers of fluorene and poly(9,9-dioctylfluorene-co-dithiophene) (F8T2). These materials may be alone or in combination.

[0123] Alternatively, the organic semiconductor layers **1017***a*, **1017***b* may be formed by using an inorganic material that is soluble in a solvent.

[0124] (v) Passivation Film **1018**

[0125] The passivation film **1018** may be formed by using, for instance, a water soluble resin such as polyvinyl alcohol (PVA), or a fluororesin.

[0126] (vii) Planarizing Film **102**

[0127] The planarizing film **102** is formed by using, for instance, an organic compound such as polyimide, polyamide, and acrylic resin material.

[0128] (viii) Anode **103**

[0129] The anode **103** is made of a metal material containing silver (Ag) or aluminum (Al). Further, in a top-emission type display panel such as the organic EL display panel **10** pertaining to the present embodiment, it is desirable that a surface portion of the anode **103** have high reflectivity.

[0130] (ix) Light-Transmissive Conduction Film **104**

[0131] The light-transmissive conduction film **104** is formed by using, for instance, Indium Tin Oxide (ITO), Indium Zinc Oxide (IZO), or the like.

[0132] (x) Hole Injection Layer **105**

[0133] The hole injection layer **105** is a layer made of, for instance, an oxide of a metal such as silver (Ag), molybdenum (Mo), chromium (Cr), vanadium (V), tungsten (W), nickel (Ni), and iridium (Ir), or a conductive polymer material such as PEDOT (an amalgam of polythiophene and polystyrene sulfonic acid). The hole injection layer **105** in the organic EL display panel **10** pertaining to the present embodiment as illustrated in FIG. **2** is assumed to be made of a metal oxide. In such a case, the hole injection layer **105** is provided with a function of assisting hole generation and injecting holes into the organic light-emitting layer **108** with a higher level of stability, compared to when the hole injection layer **105** is made of a conductive polymer material such as PEDOT. As such, the hole injection layer **105**, when made of a metal oxide, has a higher work function than the hole injection layer **105**, when made of a conductive polymer material.

[0134] Here, a case where the hole injection layer **105** is made of an oxide of a transition metal is considered. In such a case, a plurality of levels can be occupied since there are a plurality of oxidation numbers. This makes hole injection easy and allows for reduction of driving voltage. It is particularly desirable to form the hole injection layer **105** by using tungsten oxide (WO_X) since the hole injection layer **105** can be provided with the function of stably injecting holes and assisting the generation of holes.

[0135] (xi) Banks **106**

[0136] The banks **106** are formed by using an organic material such as resin and have insulative properties. Example of organic material usable for forming the banks **106** include acrylic resins, polyimide resins, and novolac type phenolic resin. In addition, it is desirable that the banks **106** have organic solvent resistance. Further, since the banks **106** may undergo processes such as etching, baking, etc. when being formed, it is desirable that the banks **106** be formed from highly resistant material that will not change excessively in shape or quality during such processes. In addition, to provide the banks **106** with liquid repellency, the surfaces thereof can be fluoridated.

[0137] This is since, if a liquid-philic material is used to form the banks **106**, the difference in liquid philicity/liquid repellency between the surfaces of the banks **106** and the surface of organic light-emitting layer **108** becomes small, and it thus becomes difficult to keep ink including an organic substance for forming the organic light-emitting layer **108** to be selectively held within the apertures defined by the banks **106**.

[0138] In addition, the banks **106** need not be formed so as to have a single-layer structure as shown in FIG. **2**. That is, the banks **106** may be alternatively formed so as to have a structure including two or more layers. In such a case, the above materials may be combined for each layer, or layers may alternate between inorganic and organic material.

[0139] (xii) Hole Transport Layer **107**

[0140] The hole transport layer **107** is formed by using a high-molecular compound not containing a hydrophilic group. For instance, the hole transport layer **107** may be formed by using a high-molecular compound such as polyfluorene or a derivative thereof, and polyallylamine or a derivative thereof, but not containing a hydrophilic group.

[0141] (xiii) Organic Light-Emitting Layer **108**

[0142] The organic light-emitting layer **108** has a function of emitting light when an excitation state is produced by the recombination of holes and electrons injected thereto. It is desirable that material used to form the organic light-emitting

layer **108** is a light emitting-organic material, a film of which can be formed by wet printing.

[0143] Specifically, it is desirable that the organic light-emitting layer **108** be formed from a fluorescent material such as an oxinoid compound, perylene compound, coumarin compound, azacoumarin compound, oxazole compound, oxadiazole compound, perinone compound, pyrrolo-pyrrole compound, naphthalene compound, anthracene compound, fluorene compound, fluoranthene compound, tetracene compound, pyrene compound, coronene compound, quinolone compound and azaquinolone compound, pyrazoline derivative and pyrazolone derivative, rhodamine compound, chrysene compound, phenanthrene compound, cyclopentadiene compound, stilbene compound, diphenylquinone compound, styryl compound, butadiene compound, dicyanomethylene pyran compound, dicyanomethylene thiopyran compound, fluorescein compound, pyrylium compound, thiapyrylium compound, selenapyrylium compound, telluropyrylium compound, aromatic aldadiene compound, oligophenylene compound, thioxanthene compound, anthracene compound, cyanine compound, acridine compound, metal complex of a 8-hydroxyquinoline compound, metal complex of a 2-bipyridine compound, complex of a Schiff base and a group three metal, metal complex of oxine, rare earth metal complex, etc., as recited in Japanese Patent Application Publication No. H5-163488.

[0144] (xiv) Electron Transport Layer **109**

[0145] The electron transport layer **110** has a function of transporting electrons injected through the cathode **111** to the organic light-emitting layer **108**, and is formed by using, for instance, an oxadiazole derivative (OXD), a triazole derivative (TAZ), a phenanthroline derivative (BCP, Bphen), or the like.

[0146] (xv) Cathode **110**

[0147] The cathode **110** is formed by using, for instance, Indium Tin Oxide (ITO), Indium Zinc Oxide (IZO), or the like. Further, in a top-emission type display panel such as the organic EL display panel **10** pertaining to the present embodiment, it is desirable that the cathode **110** be formed by using light-transmissive material. When forming the cathode **111** by using light-transmissive material as described above, it is desirable that the cathode **111** be provided with light-transmissivity of 80% or greater.

[0148] In addition to the materials presented above, the following materials may be used to form the cathode **110**. That is, the cathode **110** may be formed, for instance, as a layer including an alkali metal, a layer including an alkali earth metal, or a layer including an alkali earth metal halide. Alternatively, the cathode **110** may be formed as a laminate including one of the above-described layers and a layer including Ag laminated in the stated order. When the cathode **110** is formed as a laminate as described above, the layer including Ag may be formed with Ag alone, or with an alloy of Ag. Further, in order to enhance the efficiency with which light is guided out from the organic EL display panel **10**, a highly light-transmissive, refraction index adjustment layer may be provided above the layer including Ag.

[0149] (xvi) Sealing Layer **111**

[0150] The sealing layer **111** has a function of preventing organic layers such as the organic light-emitting layer **108** from being exposed to water and/or air and is formed by using, for example, material such as silicon nitride (SiN) and silicon oxynitride (SiON). In addition, a sealing resin layer made of a resin material such as acrylic resin and silicone resin may be further disposed above the sealing layer, which is formed by using material such as silicon nitride (SiN) and silicon oxynitride (SiON) as described above.

[0151] Further, in a top-emission type display panel such as the organic EL display panel **10** pertaining to the present embodiment, it is desirable that the sealing layer **111** be formed by using light-transmissive material.

4. Arrangement of Source Electrodes **1014***a*, **1014***b*, Drain Electrodes **1014***c*, **1014***d*, and Liquid-Philic Layers **1019***a*, **1019***b* in TFT Substrate **101**

[0152] In the following, description is provided on a positional arrangement of the source electrodes **1014***a*, **1014***b* and the drain electrodes **1014***c*, **1014***d* in the TFT substrate **101**, with reference to FIG. **3**.

[0153] As illustrated in FIG. **3**, at the bottom portion of the aperture **1016***b* defined by the partition walls **1016**, the source electrode **1014***a* and the drain electrode **1014***c* are arranged such that centers, in the Y axis direction, of the source electrode **1014***a* and the drain electrode **1014***c* coincide with a center L_1 of the aperture **1016***b* in the Y axis direction. Similarly, at the bottom portion of the aperture **1016***c* defined by the partition walls **1016**, the source electrode **1014***b* and the drain electrode **1014***d* are arranged such that centers, in the Y axis direction, of the source electrode **1014***b* and the drain electrode **1014***d* coincide with a center L_1 of the aperture **1016***b* in the Y axis direction.

[0154] Further, in the aperture **1016***b*, the liquid-philic layer **1019***a* is arranged to be offset with respect to the source electrode **1014***a* and the drain electrode **1014***c*. More specifically, the liquid-philic layer **1019***a* is located upwards in the Y axis direction with respect to the source electrode **1014***a* and the drain electrode **1014***c* and so as to be apart from the source electrode **1014***a* and the drain electrode **1014***c*. In other words, in the aperture **1016***b*, a center of area of the liquid-philic layer **1019***a* is offset from a center of area of the aperture **1016***b* in a direction differing from the direction of the aperture **1016***a* or that is, a direction differing from the left direction along the X axis.

[0155] Similarly, in the aperture **1016***c*, the liquid-philic layer **1019***b* is arranged to be offset with respect to the source electrode **1014***b* and the drain electrode **1014***d*. More specifically, the liquid-philic layer **1019***b* is located downwards in the Y axis direction with respect to the source electrode **1014***b* and the drain electrode **1014***d* and so as to be apart from the source electrode **1014***b* and the drain electrode **1014***d*. In other words, in the aperture **1016***c*, a center of area of the liquid-philic layer **1019***b* is offset from a center of area of the aperture **1016***c* in a direction differing from the direction of the aperture **1016***b* or that is, a direction differing from the left direction along the X axis.

[0156] According to the present embodiment, by disposing the liquid-philic layer **1019***a* at the bottom portion of the aperture **1016***b*, within the aperture **1016***b*, a center of a total of areas of the source electrode **1014***a*, the drain electrode **1014***c*, and the liquid-philic layer **1019***a* is offset from the center of area of the bottom portion of the aperture **1016***b* in the upper direction along the Y axis, which differs from the direction of the aperture **1016***a*. Similarly, by disposing the liquid-philic layer **1019***b* at the bottom portion of the aperture **1016***c*, within the aperture **1016***c*, a center of a total of areas of the source electrode **1014***b*, the drain electrode **1014***d*, and the liquid-philic layer **1019***b* is offset from the center of area

of the bottom portion of the aperture **1016***c* in the upper direction along the Y axis, which differs from the direction of the aperture **1016***b*.

[0157] Note that each of "a center of a total of areas of the source electrode **1014***a*, the drain electrode **1014***c*, and the liquid-philic layer **1019***a*" and "a center of a total of areas of the source electrode **1014***b*, the drain electrode **1014***d*, and the liquid-philic layer **1019***b*" as mentioned above can be calculated according to Math. 1 above.

[0158] In addition, as illustrated in FIG. **3**, at a point when the organic semiconductor layer **1017***a* has not yet been formed, at the bottom portion of the aperture **1016***b*, a center of area of the exposed portion **1013***a* of the insulating layer **1013** is offset from the center of area of the bottom portion of the aperture **1016***b* in the lower direction along the Y axis. Similarly, at a point when the organic semiconductor layer **1017***b* has not yet been formed, at the bottom portion of the aperture **1016***c*, a center of area of the exposed portion **1013***b* of the insulating layer **1013** is offset from the center of area of the bottom portion of the aperture **1016***c* in the upper direction along the Y axis.

5. Method of Manufacturing Organic Display Device 1

[0159] (i) Overview of Method of Manufacturing Organic EL Display Panel **10**

[0160] In the following, description is provided on a method of manufacturing the organic EL display device **1**, and in particular, a method of manufacturing the organic EL display panel **10**, with reference to FIG. **2** and FIGS. **4**A and **4**B.

[0161] First, as illustrated in FIG. **2** and FIG. **4**A, the substrate **1011** is prepared (Step S**1**). The substrate **1011** serves as a base of the TFT substrate **101**. Then, the TFT substrate **101** is formed by forming a thin film transistor (TFT) device on the substrate **1011** (Step S**2**).

[0162] Then, as illustrated in FIG. **2** and FIG. **4**A, the planarizing film **102**, which is made of insulative material, is formed on the TFT substrate **101** (Step S**3**). As illustrated in FIG. **2**, the planarizing film **102** has the contact hole **102***a* formed therein at an area above the connection wire **1015** in the TFT substrate **101**. Further, the planarizing film **102** is formed such that upper surfaces in the Z axis direction of portions thereof other than the contact hole **102***a* are substantially planar.

[0163] Then, the anode **103** is formed on the planarizing film **102** (Step S**4**). As illustrated in FIG. **2**, the anode **103** in the organic EL display panel **10** is formed so as to be partitioned in units of light emission (i.e., in units of subpixels). Further, the anode **103** is formed so as to have a portion that is connected to the connection wire **1015** of the TFT substrate **101** by being formed along the side surface of the planarizing film **102** defining the contact hole **102***a*.

[0164] Here, note that the anode **103** can be formed, for instance, by first forming a metal film according to the sputtering method, the vacuum vapor deposition method, or the like, and then etching the metal film so formed to obtain subpixel units.

[0165] Then, the light-transmissive conduction film **104** is formed so as to cover an upper surface of the anode **103** (Step S**5**). As illustrated in FIG. **2**, the light-transmissive conduction film **104** covers not only the upper surface of the anode **103** but also surfaces of lateral edges of the anode **103**. Further, the light-transmissive conduction film **104** also covers the upper surface of the anode **103** within the contact hole **102***a*. Note that the light-transmissive conduction film **104** can also be formed, for instance, by first forming a film according to the sputtering method, the vacuum vapor deposition method, or the like, and then etching the film so formed to obtain subpixel units.

[0166] Then, the hole injection layer **105** is formed on the light-transmissive conduction film **104** (Step S**6**). Note that, although the hole injection layer **105** is formed so as to cover the entire light-transmissive conduction film **104** in FIG. **2**, the hole injection layer **105** may alternatively be formed so as to be partitioned into subpixel units.

[0167] Further, when forming the hole injection layer **105** by using a metal oxide (e.g., tungsten oxide), the formation of the metal oxide film can be performed according to specific film forming conditions. For instance, the metal oxide film can be formed under film forming conditions such that: (i) a gas including argon gas and oxygen gas is used as a sputtering gas in a chamber of a sputtering device for forming the metal oxide film; (ii) a total pressure of the sputtering gas is higher than 2.7 Pa and lower than or equal to 7.0 Pa; (iii) a partial pressure of the oxygen gas in the sputtering gas is at least 50% and at most 70%; and (iv) an input power density per unit area of the sputtering target is at least 1.0 W/cm^2 and at most 2.8 W/cm^2.

[0168] Then, the banks **106** defining subpixels of the organic EL display panel **10** are formed (Step S**7**). As illustrated in FIG. **2**, the banks **106** are formed so as to be layered onto the hole injection layer **105**.

[0169] In specific, the banks **106** are formed by first forming a layer of material for forming the banks **106** (hereinafter referred to as a "material layer") on the hole injection layer **105**. The material layer is formed, for instance, by using a material including a photosensitive resin component and a fluorine component such as acrylic resin, polyimide resin, and novolac-type phenolic resin, and according to the spin coating method, or the like. Note that, in the present embodiment, a negative photosensitive material manufactured by Zeon Corporation (product code: ZPN 1168), which is one example of a photosensitive resin material, can be used for forming the material layer. Subsequently, by patterning the material layer so formed, apertures corresponding to the subpixels of the organic EL display panel **10** are formed. The forming of the apertures can be performed by disposing a mask onto the surface of the material layer, performing exposure from over the mask, and finally performing developing.

[0170] Then, in each concavity on the hole injection layer **105** defined by the banks **106**, the hole transport layer **107**, the organic light-emitting layer **108**, and the electron transport layer **109** are formed in the stated order so as to be layered one on top of another (Steps S**8** through S**10**).

[0171] The hole transport layer **107** is formed by first forming, according to the printing method, a film made of an organic compound for forming the hole transport layer **107**, and then sintering the film so formed. The organic light-emitting layer **108** is similarly formed by first forming a film according to the printing method, and then sintering the film so formed.

[0172] Then, the cathode **110** and the sealing layer **111** are layered onto the electron transport layer **109** in the stated order (Steps S**11** and S**12**). As illustrated in FIG. **2**, the cathode **110** and the sealing layer **111** are formed so as to cover the layers therebelow entirely, including top surfaces of the banks **106**.

[0173] Then, an adhesive resin material for forming the adhesion layer **112** is applied onto the sealing layer **111**, and a color filter (CF) panel having been prepared in advance is adhered onto the sealing layer **111** via the adhesive layer **112** (Step S**13**). As illustrated in FIG. **2**, the CF substrate **113** adhered onto the sealing layer **111** via the adhesion layer **112** includes the substrate **1131**, and the color filter **1132** and the black matrix **1133** formed on the surface of the substrate **1131** that is located lower in the Z axis direction.

[0174] As such, the manufacturing of the organic EL display panel **10**, which is an organic EL display element, is completed.

[0175] Note that, although illustration is not provided in the drawings, the manufacturing of the organic EL display device **1** is completed by annexing the drive control circuit portion **20** to the organic EL display panel **10** (refer to FIG. **1**), and then performing aging processing. The aging processing is performed by, for instance, causing the organic EL display device **1** to conduct until the mobility of holes in the organic EL display device **1** reaches 1/10 or lower with respect to the hole injection characteristics before the aging processing. More specifically, in the aging processing, the organic EL display device **1** is electrified for a predetermined time period while maintaining the luminous intensity of the organic EL display device **1** to be at least equal to the luminous intensity upon actual usage and at most three times the luminous intensity upon actual usage.

[0176] (ii) Method of Foaming TFT Substrate **101**

[0177] Subsequently, description is provided on a method of forming the TFT substrate **101**, with reference to FIG. **4**B, FIG. **3**, FIGS. **5**A through **5**C, FIGS. **6**A through **6**C, FIGS. **7**A through **7**C, and FIGS. **8**A and **8**B.

[0178] As illustrated in FIG. **5**A, the gate electrodes **1012***a*, **1012***b* are formed on a main surface of the substrate **1011** (Step S**21** in FIG. **4**B). Note that the formation of the gate electrodes **1012***a*, **1012***b* may be performed according to the above-described method applied in the formation of the anode **103**.

[0179] Then, as illustrated in FIG. **5**B, the insulating layer **1013** is formed so as to cover the substrate **1011** and the gate electrodes **1012***a*, **1012***b* (Step S**22** in FIG. **4**B). Then, as illustrated in FIG. **5**C, the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the connection wire **1015** are formed on a main surface of the insulating layer **1013** (Step S**23** in FIG. **4**B). Further, the liquid-philic layers **1019***a*, **1019***b* are formed in the same step in accordance with the positional arrangement illustrated in FIG. **3**.

[0180] In this step, note that the positions of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the liquid-philic layers **1019***a*, **1019***b* with respect to the insulating layer **1013** are defined such that (i) the relative position of the liquid-philic layer **1019***a* with respect to the source electrode **1014***a* and the drain electrode **1014***c*, and (ii) the relative position of the liquid-philic layer **1019***b* with respect to the source electrode **1014***b* and the drain electrode **1014***d* are in accordance with the positional relationships illustrated in FIG. **3**. Such arrangements are made in the present step taking into account the partition walls **1016** that are formed through the following steps. Further, as illustrated in FIG. **3**, the exposed portion **1013***a* is formed at the lower side of the aperture **1016***b* in the Y axis direction, and similarly, the exposed portion **1013***b* is formed at the upper side of the aperture **1016***c* in the Y axis direction.

[0181] Then, as illustrated in FIG. **6**A, a film **10160** of photoresist material for forming the partition walls **1016** is deposited so as to accumulate and cover the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, the connection wire **1015**, the liquid-philic layers **1019***a*, **1019***b* (undepicted in FIG. **6**A), and the exposed portions **1013***a*, **1013***b* (Step S**24** in FIG. **4**B). Then, as illustrated in FIG. **6**B, a mask **501** is disposed above the film **10160** so deposited, and mask exposure and patterning of the photoresist material film **10160** is performed (Step S**25** in FIG. **4**B). Here, note that the mask **501** has window portions **501***a*, **501***b*, **501***c*, and **501***d* formed therein which correspond in position to the partition walls **1016** to be formed. Note that, although not illustrated in FIG. **6**B, the mask **501** has additional window portions formed therein which also correspond in position to the partition walls **1016** to be formed.

[0182] The partition walls **1016**, illustration of which is provided in FIG. **6**C, are formed in such a manner as described above (Step S**26** in FIG. **4**B). The partition walls **1016** define a plurality of apertures including the apertures **1016***a*, **1016***b*, and **1016***c*. More specifically, the partition walls **1016** defining the aperture **1016***a* surround the connection wire **1015**, the partition walls **1016** defining the aperture **1016***b* surround the source electrode **1014***a*, the drain electrode **1014***c*, and the liquid-philic layer **1019***a*, and the partition walls **1016** defining the aperture **1016***c* surround the source electrode **1014***b*, the drain electrode **1014***d*, and the liquid-philic layer **1019***b*. Further, within the aperture **1016***b*, the source electrode **1014***a*, the drain electrode **1014***c*, and the liquid-philic layer **1019***a* are arranged in accordance with the positional relationship illustrated in FIG. **3**, and similarly, within the aperture **1016***c*, the source electrode **1014***b*, the drain electrode **1014***d*, and the liquid-philic layer **1019***b* are arranged in accordance with the positional relationship illustrated in FIG. **3**.

[0183] After the partition walls **1016** are formed, organic semiconductor ink **10170***a*, **10170***b*, for respectively forming the organic semiconductor layers **1017***a*, **1017***b*, are respectively applied to the apertures **1016***b*, **1016***c* defined by the partition walls **1016**, as illustrated in FIG. **7**A (Step S**27** in FIG. **4**B). Here, it should be noted that a plan view surface of the organic semiconductor ink **10170***a* applied with respect to the aperture **1016***b* and a plan view surface of the organic semiconductor ink **10170***a* applied with respect to the aperture **1016***b* are not symmetric in the X axis direction in FIG. **7**A. Rather, the plan view surface of the organic semiconductor ink **10170***a* and the plan view surface of the organic semiconductor ink **10170***a* are off-center in different directions (the directions indicated by arrows F_1 and F_2 in FIG. **7**A).

[0184] More specifically, as illustrated in FIG. **7**B, the surface shape of the organic semiconductor ink **10170***a* applied with respect to the aperture **1016***b* is biased in one direction along the Y axis (i.e., the direction indicated by the arrow F_1 illustrated above the organic semiconductor ink **10170***a*). In other words, the organic semiconductor ink **10170***a* applied with respect to the aperture **1016***b* has a shape such that one side along the Y axis in the direction indicated by the arrow F_1 includes a greater distribution of portions having relatively great surface height than the other side. On the other hand, as illustrated in FIG. **7**C, the surface shape of the organic semiconductor ink **10170***b* applied with respect to the aperture **1016***c* is biased in one direction along the Y axis (i.e., the direction indicated by the arrow F_2 illustrated above the

organic semiconductor ink **10170***b*). In other words, the organic semiconductor ink **10170***b* applied with respect to the aperture **1016***c* has a shape such that one side along the Y axis in the direction indicated by the arrow F_2 includes a greater distribution of portions having relatively great surface height than the other side.

[0185] By controlling the surface shapes of the organic semiconductor ink **10170***a*, **10170***b* in such a manner, the organic semiconductor ink **10170***a*, **10170***b* is (i) prevented from overflowing and flowing out towards undesirable areas including the aperture **1016***a*, and (ii) prevented from meeting and blending with each other. The specific reasons as to why such problems can be prevented are described later in the present disclosure.

[0186] Subsequently, by drying the organic semiconductor ink **10170***a*, **10170***b* (Step S**28** in FIG. **4**B), the organic semiconductor layers **1017***a*, **1017***b* are respectively formed with respect to the apertures **1016***b*, **1016***c* (Step S**29** in FIG. **4**B).

[0187] Finally, the formation of the TFT substrate **101** is completed by forming the passivation film **1018** so as to entirely cover underlayers therebelow with the exception of a contact area including the aperture **1016***a*, etc., as illustrated in FIG. **8**B (Step S**30** in FIG. **4**B).

6. Effects Achieved

[0188] For the reasons explained in the following, the TFT substrate **101** pertaining to the present embodiment, the organic EL display panel **10** including the TFT substrate **101**, and the organic EL display device **1** having a structure including the organic EL display panel **10** are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0189] As illustrated in FIGS. **7**A through **7**C, according to the TFT substrate **101** pertaining to the present embodiment, when the organic semiconductor ink **10170***a*, **10170***b*, which are for respectively forming the organic semiconductor layers **1017***a*, **1017***b*, are respectively applied with respect to the apertures **1016***b*, **1016***c*, the organic semiconductor ink **10170***a* exhibits a shape such that the above-described side thereof, which is not in the direction along which the aperture **1016***a* adjacent to the aperture **1016***b* exists, includes a great distribution of portions having great surface height. More specifically, the side of the organic semiconductor ink **10170***a* in the direction indicated by the arrow F_1 in FIGS. **7**A and **7**B includes portions having great surface height. Due to this, it is unlikely that the organic semiconductor ink **10170***a* flows out towards the aperture **1016***a*.

[0190] In addition, when comparing the organic semiconductor ink **10170***a* applied with respect to the aperture **1016***b* and the organic semiconductor ink **10170***b* applied with respect to the aperture **1016***c*, portions having great surface height are located at opposite sides along the Y axis direction, as indicated by the arrows F_1 and F_2 in FIGS. **7**A through **7**C. Due to this, it is unlikely that the organic semiconductor ink **10170***a* and the organic semiconductor ink **10170***b* meet and blend with each other.

[0191] As such, in the TFT substrate **101** pertaining to the present embodiment, the formation of the organic semiconductor layers **1017***a*, **1017***b* at only desired areas (i.e., the channel portions) is realized. In addition, by preventing the organic semiconductor ink **10170***a*, **10170***b* from overflowing, the layer thicknesses of the organic semiconductor layers **1017***a* and **1017***b* (i.e., the layer thickness of an organic semiconductor layer **1017**) can be controlled with high precision. Furthermore, high performance is guaranteed of each of a thin film transistor element formed at an area corresponding to the aperture **1016***b* and a thin film transistor element formed at an area corresponding to the aperture **1016***c*.

[0192] As such, the TFT substrate **101** pertaining to the present embodiment, the organic EL display panel **10** including the TFT substrate **101**, and the organic EL display device **1** having a structure including the organic EL display panel **10**, upon formation of the organic semiconductor layer **1017** in the TFT substrate **101**, (i) prevents the formation of the organic semiconductor layer **1017** at undesirable areas, and (ii) prevents the organic semiconductor ink **10170***a*, **10170***b* from meeting and blending with each other, and thereby ensures high quality.

[0193] Note that the above-described effect is a result of (i) the positional arrangement of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the liquid-philic layers **1019***a*, **1019***b* at the bottom portion of the apertures **1016***b*, **1016***c*, and (ii) a specific relationship between the liquid repellency of the surfaces of the partition walls **1016**, the liquid repellency of the surface of the insulating layer **1013**, and the liquid repellency of the surfaces of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the liquid-philic layers **1019***a*, **1019***b*. In specific, the following relationship is satisfied when denoting: the liquid repellency of the surfaces of the partition walls **1016** as R_W; the liquid repellency of the surface of the insulating layer **1013** as R_1; and the liquid repellency of the surfaces of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the liquid-philic layers **1019***a*, **1019***b* as R_E.

$$R_W > R_I > R_E \quad \text{[Math. 2]}$$

[0194] Note that, the liquid repellency denoted by each of R_W, R_I, and R_E indicates the liquid repellency of the corresponding surface(s) with respect to the organic semiconductor ink **10170***a*, **10170***b*.

[0195] In the meantime, when seen from an opposite point of view, or that is, in terms of wettability, the characteristics of the surfaces of the partition walls **1016**, the characteristics of the surface of the insulating layer **1013**, and the characteristics of the surfaces of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the liquid-philic layers **1019***a*, **1019***b* satisfy the following relationship.

$$W_W < W_I < W_E \quad \text{[Math. 3]}$$

[0196] In Math. 3, W_W denotes the wettability of the surfaces of the partition walls **1016**, W_1 denotes the wettability of the surface of the insulating layer **1013**, and W_E denotes the wettability of the surfaces of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the liquid-philic layers **1019***a*, **1019***b*.

[0197] As described up to this point, according to the present embodiment, control is performed of (i) the positional arrangement of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, the liquid-philic layers **1019***a*, **1019***b* at the bottom portion of the apertures **1016***b*, **1016***c*, and (ii) the relationship between the liquid repellency of the surfaces of the partition walls **1016**, the liquid repellency of the surface of the insulating layer **1013**, and the liquid repellency of the surfaces of the source electrodes **1014***a*, **1014***b*, the drain electrodes **1014***c*, **1014***d*, and the liquid-philic layers **1019***a*, **1019***b*. Due to this, the surfaces of the organic semiconductor ink **10170***a*, **10170***b*, upon application in the manufacturing of the TFT substrate **101**, exhibit the shapes as illustrated in FIGS. **7**A through **7**C. Hence, the organic semi-

conductor ink **10170***a*, **10170***b* can be (i) effectively prevented from overflowing and flowing out towards undesirable areas such as the inside of the aperture **1016***a* and (ii) effectively prevented from meeting and blending with each other. This results in the formation of the organic semiconductor layers **1017***a*, **1017***b* at undesirable portions being prevented and the degradation of device characteristics due to meeting and blending of organic semiconductor ink between thin film transistor elements being prevented. As such, the TFT substrate **101**, the organic EL display panel **10**, and the organic EL display device **1** are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0198] Note that, as illustrated in FIG. **3**, the exposed portions **1013***a*, **1013***b* are formed by the liquid-philic layers **1019***a*, **1019***b* being disposed at the bottom portions of the apertures **1016***b*, **1016***c*. As a result, at the bottom portion of the aperture **1016***b*, the area of the insulating layer **1013** remaining exposed is greater at the lower side of the bottom portion in the Y axis direction than at the upper side. On the other hand, at the bottom portion of the aperture **1016***c*, the area of the insulating layer **1013** remaining exposed is greater at the upper side of the bottom portion in the Y axis direction than at the lower side. Such a relationship is also effective in achieving the above-described effects.

Embodiment 2

[0199] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 2 of the present disclosure, with reference to FIG. **9**A. FIG. **9**A corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **9**A and FIG. **3**, embodiment 2 is similar to embodiment 1. As such, the structures similar between embodiment 2 and embodiment 1 are not illustrated in the drawings nor will be described in the following.

[0200] As illustrated in FIG. **9**A, the TFT substrate pertaining to the present embodiment has partition walls **2016** that define four apertures, namely apertures **2016***a*, **2016***b*, **2016***c*, **2016***d*. Among the four apertures that are defined by the partition walls **2016**, the apertures **2016***a*, **2016***d* are respectively provided with connection wires **2015***a*, **2015***b* at bottom portions thereof, and thus, do not function as channel portions.

[0201] Note that, as illustrated in FIG. **9**A, one of the apertures **2016***a*, **2016***d*, which do not function as channel portions, here for instance, the aperture **2016***d* belongs to a TFT element that corresponds to a subpixel adjacent to a subpixel that the apertures **2016***a* through **2016***c* correspond to.

[0202] In addition, at the bottom portion of the aperture **2016***b*, a source electrode **2014***a*, a drain electrode **2014***c*, and liquid-philic layers **2019***a*, **2019***b* are disposed. Similarly, at the bottom portion of the aperture **2016***c*, a source electrode **2014***b*, a drain electrode **2014***d*, and liquid-philic layers **2019***c*, **2019***d* are disposed.

[0203] The source electrode **2014***a* and the drain electrode **2014***c* at the bottom portion of the aperture **2016***b*, and the source electrode **2014***b* and the drain electrode **2014***d* at the bottom portion of the aperture **2016***c* each have a square or rectangular shape. Further, one side of the source electrode **2014***a* faces one side of the drain electrode **2014***c*, and similarly, one side of the source electrode **2014***b* faces one side of the drain electrode **2014***d*.

[0204] In the present embodiment, at the bottom portion of the aperture **2016***b*, the liquid-philic layer **2019***a* is disposed upwards in the Y axis direction with respect to the drain electrode **2014***c* and so as to be apart from the drain electrode **2014***c*, and the liquid-philic layer **2019***b* is disposed downwards in the Y axis direction with respect to the drain electrode **2014***c* and so as to be apart from the drain electrode **2014***c*. Further, note that, at the bottom portion of the aperture **2016***b*, the liquid-philic layers **2019***a*, **2019***b* are disposed so as to be off-center to the right in the X axis direction.

[0205] On the other hand, at the bottom portion of the aperture **2016***c*, the liquid-philic layer **2019***c* is disposed upwards in the Y axis direction with respect to the source electrode **2014***b* and the drain electrode **2014***d* and so as to be apart from the source electrode **2014***b* and the drain electrode **2014***d*, and the liquid-philic layer **2019***d* is disposed downwards in the Y axis direction with respect to the source electrode **2014***b* and the drain electrode **2014***d* and so as to be apart from the source electrode **2014***b* and the drain electrode **2014***d*. Further, note that, at the bottom portion of the aperture **2016***c*, a center of area of each of the liquid-philic layers **2019***c*, **2019***d* coincides with a center of area of the bottom portion of the aperture **2016***b* in the X axis direction.

[0206] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **2016***b*, **2016***c*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **2016***b* is biased in the direction indicated by the arrow F_3, which differs from the direction along which the aperture **2016***a* adjacent to the aperture **2016***b* exists. On the other hand, the surface shape of the organic semiconductor ink applied with respect to the aperture **2016***c* is biased in the directions indicated by the arrows F_4 and F_5.

[0207] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0208] Note that, similar as in embodiment 1, the liquid-philic layers **2019***a*, **2019***b*, **2019***c*, **2019***d* are formed by using the same material as used for forming the source electrodes **2014***a*, **2014***b* and the drain electrodes **2014***c*, **2014***d* in the present embodiment. However, the material for forming the liquid-philic layers **2019***a*, **2019***b*, **2019***c*, **2019***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 3

[0209] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 3 of the present disclosure, with reference to FIG. **9**B. FIG. **9**B corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **9**B and FIG. **3**, embodiment 3 is similar to embodiments 1 and 2. As such, the structures similar between embodiment 3 and embodiments 1 and 2 are not illustrated in the drawings nor will be described in the following.

[0210] As illustrated in FIG. **9**B, the TFT substrate pertaining to the present embodiment has partition walls **2116** that define four apertures, namely apertures **2116***a*, **2116***b*, **2116***c*,

2116*d*. Among the four apertures that are defined by the partition walls **2116**, the apertures **2116***a*, **2116***d* are respectively provided with connection wires **2115***a*, **2115***b* at bottom portions thereof, and thus, do not function as channel portions.

[0211] Note that, as illustrated in FIG. **9**B, one of the apertures **2116***a*, **2116***d* not functioning as channel portions, here for instance, the aperture **2116***d* belongs to a TFT element that corresponds to a subpixel adjacent to a subpixel that the apertures **2116***a* through **2116***c* correspond to. This is similar as in embodiment 2.

[0212] In addition, at the bottom portion of the aperture **2116***b*, a source electrode **2114***a*, a drain electrode **2114***c*, and liquid-philic layers **2119***a*, **2119***b* are disposed. Similarly, at the bottom portion of the aperture **2116***c*, a source electrode **2114***b*, a drain electrode **2114***d*, and liquid-philic layers **2119***c*, **2119***d* are disposed.

[0213] The source electrode **2114***a* and the drain electrode **2114***c* at the bottom portion of the aperture **2116***b*, and the source electrode **2114***b* and the drain electrode **2114***d* at the bottom portion of the aperture **2116***c* each have a square or rectangular shape. Further, one side of the source electrode **2114***a* faces one side of the drain electrode **2114***c*, and similarly, one side of the source electrode **2114***b* faces one side of the drain electrode **2114***d*.

[0214] In the present embodiment, at the bottom portion of the aperture **2116***b*, the liquid-philic layer **2119***a* is disposed upwards in the Y axis direction with respect to the source electrode **2114***a* and the drain electrode **2114***c* and so as to be apart from the source electrode **2114***a* and the drain electrode **2114***c*, and the liquid-philic layer **2119***b* is disposed downwards in the Y axis direction with respect to the source electrode **2114***a* and the drain electrode **2114***c* and so as to be apart from the source electrode **2114***a* and the drain electrode **2114***c*. Further, note that, at the bottom portion of the aperture **2116***b*, a center of area of each of the liquid-philic layers **2119***a*, **2119***b* coincides with a center of area of the bottom portion of the aperture **2116***b* in the X axis direction.

[0215] On the other hand, at the bottom portion of the aperture **2116***c*, the liquid-philic layer **2119***c* is disposed upwards in the Y axis direction with respect to the source electrode **2114***b* and so as to be apart from the source electrode **2114***b*, and the liquid-philic layer **2119***d* is disposed downwards in the Y axis direction with respect to the source electrode **2114***b* and so as to be apart from the source electrode **2114***b*. Further, note that, at the bottom portion of the aperture **2116***c*, the liquid-philic layers **2119***c*, **2119***d* are disposed so as to be off-center to the left in the X axis direction.

[0216] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **2116***b*, **2116***c*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **2116***b* is biased in the directions indicated by the arrows F_6 and F_7, which differ from the directions along which the apertures **2116***a*, **2116***c* adjacent to the aperture **2116***b* exist. On the other hand, the surface shape of the organic semiconductor ink applied with respect to the aperture **2116***c* is biased in the direction indicated by the arrow F_8, which differs from the direction along which the aperture **2116***d* adjacent to the aperture **2116***c* exists.

[0217] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0218] Note that, similar as in embodiment 1, etc., the liquid-philic layers **2119***a*, **2119***b*, **2119***c*, **2119***d* are formed by using the same material as used for forming the source electrodes **2114***a*, **2114***b* and the drain electrodes **2114***c*, **2114***d* in the present embodiment. However, the material for forming the liquid-philic layers **2119***a*, **2119***b*, **2119***c*, **2119***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 4

[0219] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 4 of the present disclosure, with reference to FIG. **9**C. FIG. **9**C corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **9**C and FIG. **3**, embodiment 4 is similar to embodiments 1, 2, and 3. As such, the structures similar between embodiment 4 and embodiments 1, 2, and 3 are not illustrated in the drawings nor will be described in the following.

[0220] As illustrated in FIG. **9**C, the TFT substrate pertaining to the present embodiment has partition walls **2216** that define four apertures, namely apertures **2216***a*, **2216***b*, **2216***c*, **2216***d*. Among the four apertures that are defined by the partition walls **2216**, the apertures **2216***a*, **2216***d* are respectively provided with connection wires **2215***a*, **2215***b* at bottom portions thereof, and thus, do not function as channel portions.

[0221] Note that, as illustrated in FIG. **9**C, one of the apertures **2216***a*, **2216***d* not functioning as channel portions, here for instance, the aperture **2216***d* belongs to a TFT element that corresponds to a subpixel adjacent to a subpixel that the apertures **2216***a* through **2216***c* correspond to. This is similar to embodiment 2, etc.

[0222] In addition, at the bottom portion of the aperture **2216***b*, a source electrode **2214***a*, a drain electrode **2214***c*, and liquid-philic layers **2219***a*, **2219***b* are disposed. Similarly, at the bottom portion of the aperture **2216***c*, a source electrode **2214***b*, a drain electrode **2214***d*, and liquid-philic layers **2219***c*, **2219***d* are disposed.

[0223] The source electrode **2214***a* and the drain electrode **2214***c* at the bottom portion of the aperture **2216***b*, and the source electrode **2214***b* and the drain electrode **2214***d* at the bottom portion of the aperture **2216***c* each have a square or rectangular shape. Further, one side of the source electrode **2214***a* faces one side of the drain electrode **2214***c*, and similarly, one side of the source electrode **2214***b* faces one side of the drain electrode **2214***d*.

[0224] In the present embodiment, at the bottom portion of the aperture **2216***b*, the liquid-philic layer **2219***a* is disposed upwards in the Y axis direction with respect to the source electrode **2214***a* and the drain electrode **2214***c* and so as to be apart from the source electrode **2214***a* and the drain electrode **2214***c*, and the liquid-philic layer **2219***b* is disposed downwards in the Y axis direction with respect to the source electrode **2214***a* and the drain electrode **2214***c* and so as to be apart from the source electrode **2214***a* and the drain electrode

2214*c*. Further, note that, at the bottom portion of the aperture **2216***b*, a center of area of each of the liquid-philic layers **2219***a*, **2219***b* coincides with a center of area of the bottom portion of the aperture **2116***b* in the X axis direction. Further, the length of each of the liquid-philic layers **2219***a*, **2219***b* in the X axis direction is substantially half (for instance, within a range of 40% to 60%) the length of the bottom portion of the aperture **2216***b* in the X axis direction.

[0225] Similarly, at the bottom portion of the aperture **2216***c*, the liquid-philic layer **2219***c* is disposed upwards in the Y axis direction with respect to the source electrode **2214***b* and the drain electrode **2214***d* and so as to be apart from the source electrode **2214***b* and the drain electrode **2214***d*, and the liquid-philic layer **2219***d* is disposed downwards in the Y axis direction with respect to the source electrode **2214***b* and the drain electrode **2214***d* and so as to be apart from the source electrode **2214***b* and the drain electrode **2214***d*. Further, similar as described above with regards to the liquid-philic layers **2219***a*, **2219***b*, at the bottom portion of the aperture **2216***c*, a center of area of each of the liquid-philic layers **2219***c*, **2219***d* coincides with a center of area of the bottom portion of the aperture **2116***c* in the X axis direction. Further, the length of each of the liquid-philic layers **2219***c*, **2219***d* in the X axis direction is substantially half (for instance, within a range of 40% to 60%) the length of the bottom portion of the aperture **2216***c* in the X axis direction.

[0226] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **2216***b*, **2216***c*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **2216***b* is biased in the directions indicated by the arrows F_9 and F_{10}, which differ from the directions along which the apertures **2216***a*, **2216***c* adjacent to the aperture **2216***b* exist. On the other hand, the surface shape of the organic semiconductor ink applied with respect to the aperture **2216***c* is biased towards the directions indicated by the arrows F_{11} and F_{12}, which differ from the directions along which the apertures **2216***b*, **2216***d* adjacent to the aperture **2216***c* exist. Further, since the length in the X axis direction of each of the liquid-philic layers **2219***a*, **2219***b*, **2219***c*, **2219***d* is arranged to be shorter as illustrated in FIG. **9**C in the present embodiment than in embodiments 2 and 3, etc., the organic semiconductor ink applied with respect to the aperture **2216***b* and the organic semiconductor ink applied with respect to the aperture **2216***c* are prevented from meeting and blending with each other in an effective manner.

[0227] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0228] Note that, similar as in embodiment 1, etc., the liquid-philic layers **2219***a*, **2219***b*, **2219***c*, **2219***d* are formed by using the same material as used for forming the source electrodes **2214***a*, **2214***b* and the drain electrodes **2214***c*, **2214***d* in the present embodiment. However, the material for forming the liquid-philic layers **2219***a*, **2219***b*, **2219***c*, **2219***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 5

[0229] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 5 of the present disclosure, with reference to FIG. **10**A. Note that FIG. **10**A is a diagram illustrating a portion of the TFT substrate pertaining to embodiment 5.

[0230] As illustrated in FIG. **10**A, the TFT substrate pertaining to the present embodiment has partition walls **3016** that define three apertures, namely apertures **3016***a*, **3016***b*, **3016***c*. Among the three apertures that are defined by the partition walls **3016**, the aperture **3015***a* is provided with a connection wire **3015** at a bottom portion thereof, and thus, does not function as a channel portion.

[0231] On the other hand, at a bottom portion of the aperture **3016***b*, a source electrode **3014***a* and a drain electrode **3014***c* are disposed. Similarly, at a bottom portion of the aperture **3016***c*, a source electrode **3014***b* and a drain electrode **3014***d* are disposed. The source electrodes **3014***a*, **3014***b* and the drain electrodes **3014***c*, **3014***d* each have a T-shape in plan view. Further, in the aperture **3016***b*, a portion of the source electrode **3014***a* extending in the X axis direction faces a portion of the drain electrode **3014***c* extending in the X axis direction. Similarly, in the aperture **3016***c*, a portion of the source electrode **3014***b* extending in the X axis direction faces a portion of the drain electrode **3014***d* extending in the X axis direction. In addition, at the bottom portion of the aperture **3016***b*, liquid-philic layers **3019***a*, **3019***b* are disposed upwards in the Y axis direction with respect to the portion of the drain electrode **3014***c* extending in the X axis direction. Similarly, at the bottom portion of the aperture **3016***c*, liquid-philic layers **3019***c*, **3019***d* are disposed downwards in the Y axis direction with respect to the portion of the source electrode **3014***b* extending in the X axis direction.

[0232] By disposing the liquid-philic layers **3019***a*, **3019***b* in the aperture **3016***b* as described above, the surface shape of organic semiconductor ink applied with respect to the aperture **3016***b* is biased in the direction indicated by the arrow F_{13}. Similarly, by disposing the liquid-philic layers **3019***c*, **3019***d* in the aperture **3016***c* as described above, the surface shape of organic semiconductor ink applied with respect to the aperture **3016***c* is biased in the direction indicated by the arrow F_{14}. Hence, organic semiconductor ink is effectively prevented from overflowing and flowing out undesirably, and the meeting and blending of organic semiconductor ink applied with respect to adjacent apertures is effectively prevented.

[0233] The TFT substrate pertaining to the present embodiment, due to being provided with the structure described above, achieves the same effects as the structure described in embodiment 1. In addition, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0234] Note that, similar as in embodiment 1, etc., the liquid-philic layers **3019***a*, **3019***b*, **3019***c*, **3019***d* are formed by using the same material as used for forming the source electrodes **3014***a*, **3014***b* and the drain electrodes **3014***c*, **3014***d* in the present embodiment. However, the material for forming the liquid-philic layers **3019***a*, **3019***b*, **3019***c*, **3019***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 6

[0235] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 6 of the present disclosure, with reference to FIG. **10**B. Note that FIG. **10**B is a diagram illustrating a portion of the TFT substrate pertaining to embodiment 6.

[0236] As illustrated in FIG. **10**B, the TFT substrate pertaining to the present embodiment has partition walls **3116** that define three apertures, namely apertures **3116***a*, **3116***b*, **3116***c*. Among the three apertures that are defined by the partition walls **3116**, the aperture **3116***a* is provided with a connection wire **3115** at a bottom portion thereof, and thus, does not function as a channel portion.

[0237] On the other hand, at a bottom portion of the aperture **3116***b*, a source electrode **3114***a* and a drain electrode **3114***c* are disposed. Similarly, at a bottom portion of the aperture **3116***c*, a source electrode **3114***b* and a drain electrode **3114***d* are disposed. The source electrodes **3114***a*, **3114***b* and the drain electrodes **3114***c*, **3114***d* each have a comb shape in plan view and each have a comb-teeth portion. In the aperture **3116***b*, the comb teeth portion of the source electrode **3114***a* faces the comb teeth portion of the drain electrode **3114***c*. Similarly, in the aperture **3116***c*, the comb teeth portion of the source electrode **3114***b* faces the comb teeth portion of the drain electrode **3114***d*. In addition, at the bottom portion of the aperture **3116***b*, liquid-philic layers **3119***a*, **3119***b* are disposed upwards in the Y axis direction with respect to the comb-teeth portion of the drain electrode **3114***c*. Similarly, at the bottom portion of the aperture **3116***c*, liquid-philic layers **3119***c*, **3119***d* are disposed downwards in the Y axis direction with respect to the comb teeth portion of the source electrode **3114***b*.

[0238] By disposing the liquid-philic layers **3119***a*, **3119***b* in the aperture **3116***b* as described above, the surface shape of organic semiconductor ink applied with respect to the aperture **3116***b* is biased in the direction indicated by the arrow F_{15}. Similarly, by disposing the liquid-philic layers **3119***c*, **3119***d* in the aperture **3116***c* as described above, the surface shape of organic semiconductor ink applied with respect to the aperture **3116***c* is biased in the direction indicated by the arrow F_{16}. Hence, organic semiconductor ink is effectively prevented from overflowing and flowing out undesirably, and the meeting and blending of organic semiconductor ink applied with respect to adjacent apertures is effectively prevented.

[0239] The TFT substrate pertaining to the present embodiment, due to being provided with the structure described above, achieves the same effects as the structure described in embodiment 1. In addition, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0240] In addition, according to the present embodiment, the source electrodes **3114***a*, **3114***b* and the drain electrodes **3114***c*, **3114***d* each have a comb shape, and further, the comb-teeth portion of the source electrode **3114***a* faces the comb-teeth portion of the drain electrode **3114***c*, and the comb-teeth portion of the source electrodes **3114***b* faces the comb-teeth portion of the drain electrode **3114***d*. As such, the areas of the electrodes facing the corresponding electrode increase, which leads to an improvement in transistor characteristics.

[0241] Note that, similar as in embodiment 1, etc., the liquid-philic layers **3119***a*, **3119***b*, **3119***c*, **3119***d* are formed by using the same material as used for forming the source electrodes **3114***a*, **3114***b* and the drain electrodes **3114***c*, **3114***d* in the present embodiment. However, the material for forming the liquid-philic layers **3119***a*, **3119***b*, **3119***c*, **3119***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 7

[0242] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 7 of the present disclosure, with reference to FIG. **10**C. Note that FIG. **10**C is a diagram illustrating a portion of the TFT substrate pertaining to embodiment 7.

[0243] As illustrated in FIG. **10**C, the TFT substrate pertaining to the present embodiment has partition walls **3216** that define three apertures, namely apertures **3216***a*, **3216***b*, **3216***c*. The apertures **3216***a*, **3216***b*, **3216***c* each have an opening having a substantially circular shape and a bottom portion having a substantially circular shape. Among the three apertures **3216***a*, **3216***b*, **3216***c*, the aperture **3216***a* is provided with a connection wire **3215** at the bottom portion thereof, and thus, does not function as a channel portion.

[0244] On the other hand, at a bottom portion of the aperture **3216***b*, a source electrode **3214***a* and a drain electrode **3214***c* are disposed. Similarly, at a bottom portion of the aperture **3216***c*, a source electrode **3214***b* and a drain electrode **3214***d* are disposed. The source electrodes **3214***a*, **3214***b* disposed at the bottom portions of the apertures **3216***b*, **3216***c* each have a shape that is a combination of a circular portion and a rectangular portion. The drain electrodes **3214***c*, **3214***d* disposed at the bottom portions of the apertures **3216***b*, **3216***c* each have a circular arc-shaped portion.

[0245] In addition, at the bottom portion of the aperture **3216***b*, liquid-philic layers **3219***a*, **3219***b* are disposed upwards in the Y axis direction with respect to the circular arc-shaped portion of the drain electrode **3214***c*. Similarly, at the bottom portion of the aperture **3216***c*, liquid-philic layers **3219***c*, **3219***d* are disposed at the respective sides of a base portion of the rectangular portion of the source electrode **3214***b*.

[0246] By disposing the liquid-philic layers **3219***a*, **3219***b* in the aperture **3216***b* as described above, the surface shape of organic semiconductor ink applied with respect to the aperture **3216***b* is biased in the direction indicated by the arrow F_{17}. Similarly, by disposing the liquid-philic layers **3219***c*, **3219***d* in the aperture **3216***c* as described above, the surface shape of organic semiconductor ink applied with respect to the aperture **3216***c* is biased in the direction indicated by the arrow F_{18}. Hence, organic semiconductor ink is effectively prevented from overflowing and flowing out undesirably, and the meeting and blending of organic semiconductor ink applied with respect to adjacent apertures is effectively prevented.

[0247] The TFT substrate pertaining to the present embodiment, due to being provided with the structure described above, achieves the same effects as the structure described in embodiment 1. In addition, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0248] In addition, in the present embodiment, the source electrodes **3214***a*, **3214***b* and the drain electrodes **3214***c*, **3214***d* have the respective shapes as illustrated in FIG. **10**C.

As such, the areas of the electrodes facing the corresponding electrode increase, and further, a so-called "sneak current" is reduced.

[0249] Note that, similar as in embodiment 1, etc., the liquid-philic layers **3219***a*, **3219***b*, **3219***c*, **3219***d* are formed by using the same material as used for forming the source electrodes **3214***a*, **3214***b* and the drain electrodes **3214***c*, **3214***d* in the present embodiment. However, the material for forming the liquid-philic layers **3219***a*, **3219***b*, **3219***c*, **3219***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 8

[0250] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 8 of the present disclosure, with reference to FIG. **11**A. FIG. **11**A corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **11**A and FIG. **3**, embodiment 8 is similar to embodiment 1. As such, the structures similar between embodiment 8 and embodiment 1 are not illustrated in the drawings nor will be described in the following.

[0251] As illustrated in FIG. **11**A, the TFT substrate pertaining to the present embodiment has partition walls **4016** that define three apertures, namely apertures **4016***a*, **4016***b*, **4016***c*. Among the three apertures that are defined by the partition walls **4016**, the aperture **4016***a* is provided with a connection wire **4015** at a bottom portion thereof, and thus, does not function as a channel portion.

[0252] In addition, at the bottom portion of the aperture **4016***b*, a source electrode **4014***a*, a drain electrode **4014***c*, and liquid-philic layers **4019***a*, **4019***b* are disposed. Similarly, at the bottom portion of the aperture **4019***c*, a source electrode **4014***b*, a drain electrode **4014***d*, and liquid-philic layers **4019***c*, **4019***d* are disposed.

[0253] The source electrode **4014***a* and the drain electrode **4014***c* at the bottom portion of the aperture **4016***b*, and the source electrode **4014***b* and the drain electrode **4014***d* at the bottom portion of the aperture **4016***c* each have a square or rectangular shape. Further, one side of the source electrode **4014***a* faces one side of the drain electrode **4014***c*, and similarly, one side of the source electrode **4014***b* faces one side of the drain electrode **4014***d*.

[0254] In the present embodiment, at the bottom portion of the aperture **4016***b*, the liquid-philic layer **4019***a* is disposed to the left in the X axis direction with respect to the drain electrode **4014***c* and at the upper side of the bottom portion of the aperture **4016***b* in the Y axis direction, and the liquid-philic layer **4019***b* is disposed to the right in the X axis direction with respect to the drain electrode **4014***c* and at the upper side of the bottom portion of the aperture **4016***b* in the Y axis direction. Note that, each of the liquid-philic layers **4019***a*, **4019***b* is located apart from both the source electrode **4014***a* and the drain electrode **4014***c*.

[0255] On the other hand, at the bottom portion of the aperture **4016***c*, the liquid-philic layer **4019***c* is disposed to the left in the X axis direction with respect to the source electrode **4014***b* and at the lower side of the bottom portion of the aperture **4016***c* in the Y axis direction, and the liquid-philic layer **4019***d* is disposed to the right in the X axis direction with respect to the source electrode **4014***b* and at the lower side of the bottom portion of the aperture **4016***b* in the Y axis direction. Note that, each of the liquid-philic layers **4019***c*, **4019***d* is located apart from both the source electrode **4014***b* and the drain electrode **4014***d*.

[0256] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **4016***b*, **4016***c*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **4016***b* is biased in the direction indicated by the arrow F_{19}, which differs from the direction along which the aperture **4016***a* adjacent to the aperture **4016***b* exists. On the other hand, the surface shape of the organic semiconductor ink applied with respect to the aperture **4016***c* is biased in the direction indicated by the arrow F_{20}, which differs from the direction along which the aperture **4016***b* adjacent to the aperture **4016***c* exists.

[0257] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0258] Note that, similar as in embodiment 1, etc., the liquid-philic layers **4019***a*, **4019***b*, **4019***c*, **4019***d* are formed by using the same material as used for forming the source electrodes **4014***a*, **4014***b* and the drain electrodes **4014***c*, **4014***d* in the present embodiment. However, the material for forming the liquid-philic layers **4019***a*, **4019***b*, **4019***c*, **4019***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 9

[0259] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 9 of the present disclosure, with reference to FIG. **11**B. FIG. **11**B corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **11**B and FIG. **3**, embodiment 9 is similar to embodiment 1. As such, the structures similar between embodiment 9 and embodiment 1 are not illustrated in the drawings nor will be described in the following.

[0260] As illustrated in FIG. **11**B, the TFT substrate pertaining to the present embodiment has partition walls **4116** that define three apertures, namely apertures **4116***a*, **4116***b*, **4116***c*. Among the three apertures that are defined by the partition walls **4116**, the aperture **4116***a* is provided with a connection wire **4115** at a bottom portion thereof, and thus, does not function as a channel portion.

[0261] In addition, at the bottom portion of the aperture **4116***b*, a source electrode **4114***a*, a drain electrode **4114***c*, and liquid-philic layers **4119***a*, **4119***b* are disposed. Similarly, at the bottom portion of the aperture **4116***c*, a source electrode **4114***b*, a drain electrode **4114***d*, and liquid-philic layers **4119***c*, **4119***d* are disposed.

[0262] The drain electrode **4114***c* disposed in the aperture **4116***b* and the drain electrode **4114***d* disposed in the aperture **4116***c* each have a shape of an elongated rectangle whose long sides extend in the X axis direction. The drain electrode **4114***c* is in contact with the side surface portion of the partition walls **4116** facing the aperture **4116***b* at a right side thereof in the X axis direction, and the drain electrode **4114***d*

is in contact with the side surface portion of the partition walls **4116** facing the aperture **4116***d* at a left side thereof in the X axis direction.

[0263] Further, the source electrode **4114***a* disposed in the aperture **4116***b* and the source electrode **4114***b* disposed in the aperture **4116***c* each have a U-shape in plan view. Due to the source electrode **4114***a* having a U-shape as described above, the source electrode **4114***a* faces a part of the drain electrode **4114***c* at three side thereof, and similarly, due to the source electrode **4114***b* having a U-shape as described above, the source electrode **4114***b* faces a part of the drain electrode **4114***d* at three sides thereof. In addition, the source electrode **4114***a* is in contact with the side surface portion of the partition walls **4116** facing the aperture **4116***b* at upper and lower sides thereof in the Y axis direction, and the source electrode **4114***b* is in contact with the side surface portion of the partition walls **4116** facing the aperture **4116***d* at upper and lower sides thereof in the Y axis direction.

[0264] In the present embodiment, at the bottom portion of the aperture **4116***b*, the liquid-philic layer **4119***a* is disposed to the left in the X axis direction with respect to the source electrode **4114***a* and at the upper side of the bottom portion of the aperture **4116***b* in the Y axis direction, and the liquid-philic layer **4119***b* is disposed to the right in the X axis direction with respect to the source electrode **4114***a* and at the upper side of the bottom portion of the aperture **4116***b* in the Y axis direction. Note that, each of the liquid-philic layers **4119***a*, **4119***b* is located apart from both the source electrode **4114***a* and the drain electrode **4114***c*.

[0265] On the other hand, at the bottom portion of the aperture **4116***c*, the liquid-philic layer **4119***c* is disposed to the left in the X axis direction with respect to the source electrode **4114***b* and at the lower side of the bottom portion of the aperture **4116***c* in the Y axis direction, and the liquid-philic layer **4119***d* is disposed to the right in the X axis direction with respect to the source electrode **4114***b* and at the lower side of the bottom portion of the aperture **4116***b* in the Y axis direction. Note that, each of the liquid-philic layers **4119***c*, **4119***d* is located apart from both the source electrode **4114***b* and the drain electrode **4114***d*.

[0266] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **4116***b*, **4116***c*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **4116***b* is biased in the direction indicated by the arrow F_{21}, which differs from the direction along which the aperture **4116***a* adjacent to the aperture **4116***b* exists. On the other hand, the surface shape of the organic semiconductor ink applied with respect to the aperture **4116***c* is biased in the direction indicated by the arrow F_{22}, which differs from the direction along which the aperture **4116***b* adjacent to the aperture **4116***c* exists.

[0267] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0268] Note that, similar as in embodiment 1, etc., the liquid-philic layers **4119***a*, **4119***b*, **4119***c*, **4119***d* are formed by using the same material as used for forming the source electrodes **4114***a*, **4114***b* and the drain electrodes **4114***c*, **4114***d* in the present embodiment. However, the material for forming the liquid-philic layers **4119***a*, **4119***b*, **4119***c*, **4119***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 10

[0269] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 10 of the present disclosure, with reference to FIG. **11**C. FIG. **11**C corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **11**C and FIG. **3**, embodiment 10 is similar to embodiment 1. As such, the structures similar between embodiment 10 and embodiment 1 are not illustrated in the drawings nor will be described in the following.

[0270] As illustrated in FIG. **11**C, the TFT substrate pertaining to the present embodiment has partition walls **4216** that define three apertures, namely apertures **4216***a*, **4216***b*, **4216***c*. Among the three apertures that are defined by the partition walls **4216**, the aperture **4216***a* is provided with a connection wire **4215** at a bottom portion thereof, and thus, does not function as a channel portion.

[0271] In addition, at the bottom portion of the aperture **4216***b*, a source electrode **4214***a*, a drain electrode **4214***c*, and liquid-philic layers **4219***a*, **4219***b* are disposed. Similarly, at the bottom portion of the aperture **4219***c*, a source electrode **4214***b*, a drain electrode **4214***d*, and liquid-philic layers **4219***c*, **4219***d* are disposed.

[0272] The source electrode **4214***a* and the drain electrode **4214***c* disposed in the aperture **4216***b*, and the source electrode **4214***b* and the drain electrode **4214***d* disposed in the aperture **4216***c* each have a shape of an elongated rectangle whose long sides extend in the Y axis direction. In addition, each of the source electrode **4214***a* and the drain electrode **4214***c* is in contact with the side surface portion of the partition walls **4216** facing the aperture **4216***b* at upper and lower sides thereof in the Y axis direction, and each of the source electrode **4214***b* and the drain electrode **4214***d* is in contact with the side surface portion of the partition walls **4216** facing the aperture **4216***c* at upper and lower sides thereof in the Y axis direction.

[0273] In the present embodiment, at the bottom portion of the aperture **4216***b*, the liquid-philic layer **4219***a* is disposed to the left in the X axis direction with respect to the source electrode **4214***a* and at the upper side of the bottom portion of the aperture **4216***b* in the Y axis direction, and the liquid-philic layer **4219***b* is disposed to the right in the X axis direction with respect to the drain electrode **4214***c* and at the upper side of the bottom portion of the aperture **4216***b* in the Y axis direction. Note that, each of the liquid-philic layers **4219***a*, **4219***b* is located apart from both the source electrode **4214***a* and the drain electrode **4214***c*. In addition, the liquid-philic layer **4219***a* has a smaller width in the X axis direction compared with the liquid-philic layer **4219***b*, and a side of the liquid-philic layer **4219***a* to the left in the X axis direction, along which the aperture **4216***a* adjacent to the aperture **4216***b* exists, is located apart from the side surface portion of the partition walls **4216** facing the aperture **4216***b*.

[0274] On the other hand, at the bottom portion of the aperture **4216***c*, the liquid-philic layer **4219***c* is disposed to the left in the X axis direction with respect to the source electrode **4214***b* and at the lower side of the bottom portion of

the aperture **4216***c* in the Y axis direction, and the liquid-philic layer **4219***d* is disposed to the right in the X axis direction with respect to the drain electrode **4214***d* and at the lower side of the bottom portion of the aperture **4216***c* in the Y axis direction. Note that, each of the liquid-philic layers **4219***c*, **4219***d* is located apart from both the source electrode **4214***b* and the drain electrode **4214***d*.

[0275] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **4216***b*, **4216***c*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **4216***b* is biased in the direction indicated by the arrow F_{23}, which differs from the direction along which the aperture **4216***a* adjacent to the aperture **4216***b* exists. On the other hand, the surface shape of the organic semiconductor ink applied with respect to the aperture **4216***c* is biased in the direction indicated by the arrow F_{24}, which differs from the direction along which the aperture **4216***b* adjacent to the aperture **4216***c* exists.

[0276] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0277] Note that, similar as in embodiment 1, etc., the liquid-philic layers **4219***a*, **4219***b*, **4219***c*, **4219***d* are formed by using the same material as used for forming the source electrodes **4214***a*, **4214***b* and the drain electrodes **4214***c*, **4214***d* in the present embodiment. However, the material for forming the liquid-philic layers **4219***a*, **4219***b*, **4219***c*, **4219***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 11

[0278] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 11 of the present disclosure, with reference to FIG. **12**A. FIG. **12**A corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **12**A and FIG. **3**, embodiment 11 is similar to embodiment 1. As such, the structures similar between embodiment 11 and embodiment 1 are not illustrated in the drawings nor will be described in the following.

[0279] As illustrated in FIG. **12**A, the TFT substrate pertaining to the present embodiment has partition walls **5016** that define five apertures, namely apertures **5016***a*, **5016***b*, **5016***c*, **5016***d*, **5016***e*. Among the five apertures that are defined by the partition walls **5016**, the apertures **5016***a*, **5016***e* are respectively provided with connection wires **5015***a*, **5015***e* at bottom portions thereof, and thus, do not function as channel portions.

[0280] Note that, as illustrated in FIG. **12**A, one of the apertures **5016***a*, **5016***e* not functioning as channel portions, here for instance, the aperture **5016***e* belongs to a TFT element that corresponds to a subpixel adjacent to a subpixel that the apertures **5016***a* through **5016***d* correspond to. This is similar as in embodiment 2, etc.

[0281] In addition, at the bottom portion of the aperture **5016***b*, a source electrode **5014***a*, a drain electrode **5014***d*, and a liquid-philic layer **5019***a* are disposed. At the bottom portion of the aperture **5019***c*, a source electrode **5014***b*, a drain electrode **5014***e*, and a liquid-philic layer **5019***b* are disposed. At the bottom portion of the aperture **5016***d*, a source electrode **5014***c*, a drain electrode **5014***f*, and a liquid-philic layer **5019***c* are disposed.

[0282] The source electrode **5014***a* and the drain electrode **5014***d* disposed at the bottom portion of the aperture **5016***b*, the source electrode **5014***b* and the drain electrode **5014***e* disposed at the bottom portion of the aperture **5016***c*, and the source electrode **5014***c* and the drain electrode **5014***f* disposed at the bottom portion of the aperture **5016***d* each have a square or rectangular shape. Further, one side of the source electrode **5014***a* faces one side of the drain electrode **5014***d*, one side of the source electrode **5014***b* faces one side of the drain electrode **5014***d*, and one side of the source electrode **5014***c* faces one side of the drain electrode **5014***f*.

[0283] In the present embodiment, at the bottom portion of the aperture **5016***b*, the liquid-philic layer **5019***a* is disposed upwards in the Y axis direction with respect to the source electrode **5014***a* and the drain electrode **5014***c* and so as to be apart from the source electrode **5014***a* and the drain electrode **5014***c*. At the bottom portion of the aperture **5016***c*, the liquid-philic layer **5019***b* is disposed downwards in the Y axis direction with respect to the source electrode **5014***b* and the drain electrode **5014***e* and so as to be apart from the source electrode **5014***b* and the drain electrode **5014***e*. At the bottom portion of the aperture **5016***d*, the liquid-philic layer **5019***c* is disposed upwards in the Y axis direction with respect to the source electrode **5014***c* and the drain electrode **5014***f* and so as to be apart from the source electrode **5014***c* and the drain electrode **5014***f*.

[0284] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **5016***b*, **5016***c*, **5016***d*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **5016***b* is biased in the direction indicated by the arrow F_{25}, which differs from the directions along which the apertures **5016***a*, **5016***d* adjacent to the aperture **5016***b* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **5016***c* is biased in the direction indicated by the arrow F_{26}, which differs from the directions along which the apertures **5016***b*, **5016***d* adjacent to the aperture **5016***c* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **5016***d* is biased in the direction indicated by the arrow F_{27}, which differs from the directions along which the apertures **5016***c*, **5016***e* adjacent to the aperture **5016***d* exist.

[0285] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0286] Note that, similar as in embodiment 1, etc., the liquid-philic layers **5019***a*, **5019***b*, **5019***c* are formed by using the same material as used for forming the source electrodes **5014***a*, **5014***b*, **5014***c* and the drain electrodes **5014***d*, **5014***e*, **5014***f* in the present embodiment. However, the material for forming the liquid-philic layers **5019***a*, **5019***b*, **5019***c* is not

limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 12

[0287] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 12 of the present disclosure, with reference to FIG. **12**B. FIG. **12**B corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **12**B and FIG. **3**, embodiment 12 is similar to embodiment 1. As such, the structures similar between embodiment 12 and embodiment 1 are not illustrated in the drawings nor will be described in the following.

[0288] As illustrated in FIG. **12**B, the TFT substrate pertaining to the present embodiment has partition walls **5116** that define six apertures, namely apertures **5116***a*, **5116***b*, **5116***c*, **5116***d*, **5116***e*, **5116***f*. Among the six apertures that are defined by the partition walls **5116**, the apertures **5116***a*, **5116***f* are respectively provided with connection wires **5115***a*, **5115***f* at bottom portions thereof, and thus, do not function as channel portions.

[0289] Note that, as illustrated in FIG. **12**B, one of the apertures **5116***a*, **5116***f* not functioning as channel portions, here for instance, the aperture **5116***f* belongs to a TFT element that corresponds to a subpixel adjacent to a subpixel that the apertures **5116***a* through **5116***e* correspond to. This is similar as in embodiment 2, etc.

[0290] In addition, at the bottom portion of the aperture **5116***b*, a source electrode **5114***a*, a drain electrode **5114***e*, and a liquid-philic layer **5119***a* are disposed. At the bottom portion of the aperture **5119***c*, a source electrode **5114***b*, a drain electrode **5114***f*, and a liquid-philic layer **5119***b* are disposed. At the bottom portion of the aperture **5116***d*, a source electrode **5114***c*, a drain electrode **5114***g*, and a liquid-philic layer **5119***c* are disposed. At the bottom portion of the aperture **5119***e*, a source electrode **5114***d*, a drain electrode **5114***h*, and a liquid-philic layer **5119***d* are disposed.

[0291] The source electrode **5114***a* and the drain electrode **5114***e* disposed at the bottom portion of the aperture **5116***b*, the source electrode **5114***b* and the drain electrode **5114***f* disposed at the bottom portion of the aperture **5116***c*, the source electrode **5114***c* and the drain electrode **5114***g* disposed at the bottom portion of the aperture **5116***d*, and the source electrode **5114***d* and the drain electrode **5114***h* disposed at the bottom portion of the aperture **5116***e* each have a square or rectangular shape. Further, one side of the source electrode **5114***a* faces one side of the drain electrode **5114***e*, one side of the source electrode **5114***b* faces one side of the drain electrode **5114***f*, one side of the source electrode **5114***c* faces one side of the drain electrode **5114***g*, and one side of the source electrode **5114***d* faces one side of the drain electrode **5114***h*.

[0292] In the present embodiment, at the bottom portion of the aperture **5116***b*, the liquid-philic layer **5119***a* is disposed upwards in the Y axis direction with respect to the source electrode **5114***a* and the drain electrode **5114***e* and so as to be apart from the source electrode **5114***a* and the drain electrode **5114***e*. At the bottom portion of the aperture **5116***c*, the liquid-philic layer **5119***b* is disposed downwards in the Y axis direction with respect to the source electrode **5114***b* and the drain electrode **5114***f* and so as to be apart from the source electrode **5114***b* and the drain electrode **5114***f*. At the bottom portion of the aperture **5116***d*, the liquid-philic layer **5119***c* is disposed upwards in the Y axis direction with respect to the source electrode **5114***c* and the drain electrode **5114***g* and so as to be apart from the source electrode **5114***c* and the drain electrode **5114***g*. At the bottom portion of the aperture **5116***e*, the liquid-philic layer **5119***d* is disposed downwards in the Y axis direction with respect to the source electrode **5114***d* and the drain electrode **5114***h* and so as to be apart from the source electrode **5114***d* and the drain electrode **5114***h*.

[0293] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **5116***b*, **5116***c*, **5116***d*, **5116***e*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **5116***b* is biased in the direction indicated by the arrow F_{28}, which differs from the directions along which the apertures **5116***a*, **5116***c*, **5116***d* adjacent to the aperture **5116***b* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **5116***c* is biased in the direction indicated by the arrow F_{29}, which differs from the directions along which the apertures **5116***a*, **5116***b*, **5116***e* adjacent to the aperture **5116***c* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **5116***d* is biased in the direction indicated by the arrow F_{30}, which differs from the directions along which the apertures **5116***b*, **5116***e*, **5116***f* adjacent to the aperture **5116***d* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **5116***e* is biased in the direction indicated by the arrow F_{31}, which differs from the directions along which the apertures **5116***c*, **5116***d*, **5116***f* adjacent to the aperture **5116***e* exist.

[0294] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0295] Note that, similar as in embodiment 1, etc., the liquid-philic layers **5119***a*, **5119***b*, **5119***c*, **5119***d* are formed by using the same material as used for forming the source electrodes **5114***a*, **5114***b*, **5114***c*, **5114***d* and the drain electrodes **5114***e*, **5114***f*, **5114***g*, **5114***h* in the present embodiment. However, the material for forming the liquid-philic layers **5119***a*, **5119***b*, **5119***c*, **5119***d* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

Embodiment 13

[0296] In the following, description is provided on a structure of a TFT substrate pertaining to embodiment 13 of the present disclosure, with reference to FIG. **13**. FIG. **13** corresponds to FIG. **3** in embodiment 1, and other than differences between the structures illustrated in FIG. **13** and FIG. **3**, embodiment 13 is similar to embodiment 1. As such, the structures similar between embodiment 13 and embodiment 1 are not illustrated in the drawings nor will be described in the following.

[0297] As illustrated in FIG. **13**, the TFT substrate pertaining to the present embodiment has partition walls **6016** that define seven apertures, namely apertures **6016***a*, **6016***b*, **6016***c*, **6016***d*, **6016***e*, **6016***f*, **6016***g*. Among the seven apertures that are defined by the partition walls **6016**, the apertures

6016*a*, **6016***g* are respectively provided with connection wires **6015***a*, **6015***g* at bottom portions thereof, and thus, do not function as channel portions.

[0298] Note that, as illustrated in FIG. **13**, one of the apertures **6016***a*, **6016***g* not functioning as channel portions, here for instance, the aperture **6016***g* belongs to a TFT element that corresponds to a subpixel adjacent to a subpixel that the apertures **6016***a* through **6016***f* correspond to. This is similar as in embodiment 2, etc.

[0299] In addition, at the bottom portion of the aperture **6016***b*, a source electrode **6014***a*, a drain electrode **6014***f*, and a liquid-philic layer **6019***a* are disposed. At the bottom portion of the aperture **6016***c*, a source electrode **6014***b*, a drain electrode **6014***g*, and a liquid-philic layer **6019***b* are disposed. At the bottom portion of the aperture **6016***d*, a source electrode **6014***c*, a drain electrode **6014***h*, and liquid-philic layers **6019***c*, **6019***d* are disposed. At the bottom portion of the aperture **6016***e*, a source electrode **6014***d*, a drain electrode **6014***i*, and a liquid-philic layer **6019***e* are disposed. At the bottom portion of the aperture **6016***f*, a source electrode **6014***e*, a drain electrode **6014***j*, and a liquid-philic layer **6019***f* are disposed.

[0300] The source electrode **6014***a* and the drain electrode **6014***f* disposed at the bottom portion of the aperture **6016***b*, the source electrode **6014***b* and the drain electrode **6014***g* disposed at the bottom portion of the aperture **6016***c*, the source electrode **6014***c* and the drain electrode **6014***h* disposed at the bottom portion of the aperture **6016***d*, the source electrode **6014***d* and the drain electrode **6014***i* disposed at the bottom portion of the aperture **6016***e*, and the source electrode **6014***e* and the drain electrode **6014***j* disposed at the bottom portion of the aperture **6016***f* each have a square or rectangular shape. Further, one side of the source electrode **6014***a* faces one side of the drain electrode **6014***f*, one side of the source electrode **6014***b* faces one side of the drain electrode **6014***g*, one side of the source electrode **6014***c* faces one side of the drain electrode **6014***h*, one side of the source electrode **6014***d* faces one side of the drain electrode **6014***i*, and one side of the source electrode **6014***e* faces one side of the drain electrode **6014***j*.

[0301] In the present embodiment, at the bottom portion of the aperture **6016***b*, the liquid-philic layer **6019***a* is disposed upwards in the Y axis direction with respect to the source electrode **6014***a* and the drain electrode **6014***f* and so as to be apart from the source electrode **6014***a* and the drain electrode **6014***f*. At the bottom portion of the aperture **6016***c*, the liquid-philic layer **6019***b* is disposed downwards in the Y axis direction with respect to the source electrode **6014***b* and the drain electrode **6014***g* and so as to be apart from the source electrode **6014***b* and the drain electrode **6014***g*. At the bottom portion of the aperture **6016***d*, the liquid-philic layer **6019***c* is disposed upwards in the Y axis direction with respect to the source electrode **6014***c* and the drain electrode **6014***h* and so as to be apart from the source electrode **6014***c* and the drain electrode **6014***h*, and the liquid-philic layer **6019***d* is disposed downwards in the Y axis direction with respect to the source electrode **6014***c* and the drain electrode **6014***h* and so as to be apart from the source electrode **6014***c* and the drain electrode **6014***h*. At the bottom portion of the aperture **6016***e*, the liquid-philic layer **6019***e* is disposed upwards in the Y axis direction with respect to the source electrode **6014***d* and the drain electrode **6014***i* and so as to be apart from the source electrode **6014***d* and the drain electrode **6014***i*. At the bottom portion of the aperture **6016***f*, the liquid-philic layer **6019***f* is disposed downwards in the Y axis direction with respect to the source electrode **6014***e* and the drain electrode **6014***j* and so as to be apart from the source electrode **6014***e* and the drain electrode **6014***j*.

[0302] In the manufacturing of the TFT substrate pertaining to the present embodiment that has the above-described structure, when organic semiconductor ink is applied with respect to the apertures **6016***b*, **6016***c*, **6016***d*, **6016***e*, **6016***f*, the organic semiconductor ink exhibits a state as described in the following. That is, the surface shape of the organic semiconductor ink applied with respect to the aperture **6016***b* is biased in the direction indicated by the arrow F_{32}, which differs from the directions along which the apertures **6016***a*, **6016***c*, **6016***d* adjacent to the aperture **6016***b* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **6016***c* is biased in the direction indicated by the arrow F_{33}, which differs from the directions along which the apertures **6016***a*, **6016***b*, **6016***d* adjacent to the aperture **6016***c* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **6016***d* is biased in the directions indicated by the arrows F_{34} and F_{35}, which differ from the directions along which the apertures **6016***b*, **6016***c*, **6016***e*, **6016***f* adjacent to the aperture **6016***d* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **6016***e* is biased in the direction indicated by the arrow F_{36}, which differs from the directions along which the apertures **6016***d*, **6016***f*, **6016***g* adjacent to the aperture **6016***e* exist. The surface shape of the organic semiconductor ink applied with respect to the aperture **6016***f* is biased in the direction indicated by the arrow F_{37}, which differs from the directions along which the apertures **6016***d*, **6016***e*, **6016***g* adjacent to the aperture **6016***f* exist.

[0303] As such, the structure according to the present embodiment achieves the same effects as the structure described in embodiment 1, and therefore, similar as described in embodiment 1 above, an organic EL display panel and an organic EL display device including the TFT substrate pertaining to the present embodiment are ensured to have high quality, and at the same time, to have high yield in the manufacture thereof.

[0304] Note that, similar as in embodiment 1, etc., the liquid-philic layers **6019***a*, **6019***b*, **6019***c*, **6019***d*, **6019***e*, **6019***f* are formed by using the same material as used for forming the source electrodes **6014***a*, **6014***b*, **6014***c*, **6014***d*, **6014***e* and the drain electrodes **6014***f*, **6014***g*, **6014***h*, **60141**, **6014***j* in the present embodiment. However, the material for forming the liquid-philic layers **6019***a*, **6019***b*, **6019***c*, **6019***d*, **6019***e*, **6019***f* is not limited to the above, and any material having greater liquid philicity than the insulating layer is usable.

[Other Matters]

[0305] In some of the above-described embodiments 1 through 13, description has been provided of examples where, within one side of an aperture in a direction of an adjacent aperture, a portion exists where a source electrode nor a drain electrode exists and thus, where an insulating layer is in direct contact with an organic semiconductor layer. However, the one side may include a portion of the source electrode and/or a portion of the drain electrode, provided that an area of an exposed portion of the insulating layer at each of the sides be determined in relation with a shape to be exhibited by a surface of semiconductor ink applied with respect to the aperture at each of the sides.

[0306] In the above-described embodiments 1 through 13, description has been provided by taking as an example a TFT substrate to be used in the organic EL display panel **10**. However, the TFT substrate may alternatively be used in a liquid crystal display panel, a field emission display panel, etc. Further, the TFT substrate may also be used in an electronic paper, etc.

[0307] In addition, the materials described in the above-described embodiments are mere examples of such materials that may be used. As such, other materials may be used as necessary.

[0308] In addition, as illustrated in FIG. **2**, the organic EL display panel **10** pertaining to embodiment 1 is a top-emission type organic EL display panel. However, the organic EL display panel may alternatively be a bottom-emission type organic EL display panel. In such a case, the materials to be used for forming the organic EL display panel and the layout design of the organic EL display panel may be changed as necessary.

[0309] In addition, in the above, description has been provided that the apertures defined by the partition walls each have an opening having a rectangular shape or a substantially circular shape. However, the apertures defined by the partition walls may alternatively have openings of various shapes. For instance, an aperture may have an opening having a square shape as illustrated in FIG. **14**A, or may have an opening having a shape as illustrated in FIG. **14**B composed of one side being a circular arc and three remaining sides being straight lines. In addition, an aperture may have an opening having a circular shape as illustrated in FIG. **14**C, and another aperture having the shape of a circular arc may be provided so as to partially surround the circular aperture. Needless to say, the shape of an opening of an aperture corresponding to a channel portion and the shape of an opening of an aperture corresponding to a non-channel portion are interchangeable.

[0310] In addition, in the above, description has been provided that the outflow of organic semiconductor ink toward an aperture to come in contact with an anode or the like is undesirable, and thus should be prevented. However, the outflow of organic semiconductor ink to other types of apertures may alternatively be prevented. For instance, the outflow of organic semiconductor ink towards a "repair aperture" may be prevented. Here, the repair aperture refers to an aperture that is used when a defect is found in a TFT device having been formed and the TFT device is repaired by newly forming a TFT element only with respect to a cell having a defect.

[0311] Further, in cases such as where great stress is exerted on partition walls in a TFT substrate, holes may be formed in the partition walls in order to relieve the stress exerted on the partition walls. In such cases, it is desirable that configuration be made such that organic semiconductor ink is prevented from flowing out towards the holes formed in the partition walls in order to relieve the stress exerted on the partition walls. Note that, although the formation of organic semiconductor layers with respect to the above-described holes formed in the partition walls is not problematic by itself, a problem arises when organic semiconductor ink flow out towards such holes formed in the partition walls since the amount of organic semiconductor ink remaining at areas at which the formation of organic semiconductor layers is desired decreases. As such, the outflow of organic semiconductor ink towards the above-described holes is undesirable since the control of the layer thicknesses of the organic semiconductor layers would become difficult. In other words, the outflow of organic semiconductor ink towards such holes formed in the partition walls may affect TFT performance. As such, it is desirable that measures be taken so as to prevent organic semiconductor ink from flowing out towards the above-described holes formed in the partition walls in order to relieve the stress exerted on the partition walls.

[0312] Further, in embodiments 1 through 13 above, description has been provided that the liquid-philic layers **1019***a*, **1019***b*, **2019***a*, **2019***b*, **2019***c*, **2019***d*, **2119***a*, **2119***b*, **2119***c*, **2119***d*, **2219***a*, **2219***b*, **2219***c*, **2219***d*, **3019***a*, **3019***b*, **3019***c*, **3019***d*, **3119***a*, **3119***b*, **3119***c*, **3119***d*, **3219***a*, **3219***b*, **3219***c*, **3219***d*, **4019***a*, **4019***b*, **4019***c*, **4019***d*, **4119***a*, **4119***b*, **4119***c*, **4119***d*, **4219***a*, **4219***b*, **4219***c*, **4219***d*, **5019***a*, **5019***b*, **5019***c*, **5119***a*, **5119***b*, **5119***c*, **5119***d*, **6019***a*, **6019***b*, **6019***c*, **6019***d*, **6019***e*, **6019***f* are formed by using the same metal material as the source electrodes **1014***a*, **1014***b*, **2014***a*, **2014***b*, **2114***a*, **2114***b*, **2214***a*, **2214***b*, **3014***a*, **3014***b*, **3114***a*, **3114***b*, **3214***a*, **3214***b*, **4014***a*, **4014***b*, **4114***a*, **4114***b*, **4214***a*, **4214***b*, **5014***a*, **5014***b*, **5014***c*, **5114***a*, **5114***b*, **5114***c*, **5114***d*, **6014***a*, **6014***b*, **6014***c*, **6014***d*, **6014***e* and the drain electrodes **1014***c*, **1014***d*, **2014***c*, **2014***d*, **2114***c*, **2114***d*, **2214***c*, **2214***d*, **3014***c*, **3014***d*, **3114***c*, **3114***d*, **3214***c*, **3214***d*, **4014***c*, **4014***d*, **4114***c*, **4114***d*, **4214***c*, **4214***d*, **5014***d*, **5014***e*, **5014***f*, **5114***e*, **5114***f*, **5114***g*, **5114***h*, **6014***f*, **6014***g*, **6014***h*, **6014***i*, **6014***j*. However, the material usable for forming the liquid-philic layers is not limited in this way. For instance, the liquid-philic layers may be formed by using metal material differing from the metal material used for forming the source electrodes and the drain electrodes. Alternatively, material other than metal material, such as resin material, may be used as the material for forming the liquid-philic layers. When forming the liquid-philic layers by using resin material, the insulating layer (i.e., gate insulating layer) may be formed, for instance, by using a material not including fluorine, although an insulating layer (gate insulating layer) is commonly formed by using fluorine resin.

[0313] Here, it should be noted that, the formation of the liquid-philic layers by using the same metal material used for forming the source electrodes and the drain electrodes as described in embodiments 1 through 13 above is advantageous for not bringing about an increase in procedures during manufacture, and hence, in that a reduction in manufacturing cost is realized.

[0314] In addition, description has been provided in the above on a structure including an organic semiconductor layer formed by using organic semiconductor ink. However, a similar structure may alternatively be used for a structure including an inorganic semiconductor layer formed by using inorganic semiconductor ink. In such a case, the same effects as described above can be achieved. For instance, an amorphous metal oxide semiconductor may be used as the inorganic semiconductor material. It is expected for such semiconductors to be applied to displays, electronic papers, etc., for the transparency possessed thereby.

[0315] In terms of mobility, such semiconductors are materials that may potentially realize a movability of 3 to 20 cm^2/Vs, which is desirable in high performance LCD and organic electro-luminescence (EL) displays.

[0316] Some commonly-known, representative examples of an amorphous metal oxide semiconductor include an amorphous indium zinc oxide semiconductor (a-InZnO) containing indium (In) and zinc (Zn) and an amorphous indium

gallium zinc oxide semiconductor (a-InGaZnO), which includes gallium (Ga) as a metal component in addition to indium (In) and zinc (Zn).

[0317] For details concerning such inorganic semiconductors, reference may be made to disclosure in International Application No. WO 2012/035281.

[0318] In the above, description has been provided on a structure in which the outflow of organic semiconductor ink towards a specific aperture is undesirable, and thus prevented. However, application to a structure not including such an aperture is also possible. In specific, in a structure where two or more apertures with respect to which organic semiconductor layers are to be formed are arranged adjacent to each other, partition walls may be formed such that organic semiconductor ink does not flow out from one aperture towards another. By forming such partition walls, the formation of the organic semiconductor layers can be performed while it is ensured that organic semiconductor ink for forming one organic semiconductor layer exists separately from organic semiconductor ink for forming the other organic semiconductor layer. As such, compared to a case where the formation of organic semiconductor layers is performed while applied organic semiconductor ink covers two adjacent apertures and the gap therebetween, it is easier to reduce the difference between layer thickness of an organic semiconductor layer to be formed with respect to one aperture and layer thickness of another organic semiconductor layer to be formed with respect to an adjacent aperture, and as a result, excellent semiconductor characteristics and an improvement in yield can be expected.

INDUSTRIAL APPLICABILITY

[0319] The present disclosure is applicable to a display device provided with a panel, such as an organic EL display panel, and is useful for realizing a TFT device having high quality by realizing high-definition.

REFERENCE SIGNS LIST

[0320] **1** organic EL display device
[0321] **10** organic EL display panel
[0322] **20** drive control circuit portion
[0323] **21-24** drive circuit
[0324] **25** control circuit
[0325] **101** TFT substrate
[0326] **102** planarizing film
[0327] **102***a* contact hole
[0328] **103** anode
[0329] **104** light-transmissive conduction film
[0330] **105** hole injection layer
[0331] **106** bank
[0332] **107** hole transport layer
[0333] **108** organic light-emitting layer
[0334] **109** electron transport layer
[0335] **110** cathode
[0336] **111** sealing layer
[0337] **112** adhesion layer
[0338] **113** CF substrate
[0339] **501** mask
[0340] **1011**, **1131** substrate
[0341] **1012***a*, **1012***b* gate electrode
[0342] **1013** insulating layer
[0343] **1014***a*, **1014***b*, **2014***a*, **2014***b*, **2114***a*, **2114***b*, **2214***a*, **2214***b*, **3014***a*, **3014***b*, **3114***a*, **3114***b*, **3214***a*, **3214***b*, **4014***a*, **4014***b*, **4114***a*, **4114***b*, **4214***a*, **4214***b*, **5014***a*, **5014***b*, **5014***c*, **5114***a*, **5114***b*, **5114***c*, **5114***d*, **6014***a*, **6014***b*, **6014***c*, **6014***d*, **6014***e* source electrode
[0344] **1014***c*, **1014***d*, **2014***c*, **2014***d*, **2114***c*, **2114***d*, **2214***c*, **2214***d*, **3014***c*, **3014***d*, **3114***c*, **3114***d*, **3214***c*, **3214***d*, **4014***c*, **4014***d*, **4114***c*, **4114***d*, **4214***c*, **4214***d*, **5014***d*, **5014***e*, **5014***f*, **5114***e*, **5114***f*, **5114***g*, **5114***h*, **6014***f*, **6014***g*, **6014***h*, **6014***i*, **6014***j* drain electrode
[0345] **1015**, **2015***a*, **2015***d*, **2115***a*, **2115***d*, **2215***a*, **2215***d*, **3015**, **3115**, **3215**, **4015**, **4115**, **4215**, **5015***a*, **5015***e*, **5115***a*, **5115***f*, **6015***a*, **6015***g* connection wire
[0346] **1016**, **2016**, **2116**, **2216**, **3016**, **3116**, **3216**, **4016**, **4116**, **4216**, **5016**, **5116**, **6016** partition walls
[0347] **1016***a*, **1016***b*, **1016***c*, **2016***a*, **2016***b*, **2016***c*, **2016***d*, **2116***a*, **2116***b*, **2116***c*, **2116***d*, **2216***a*, **2216***b*, **2216***c*, **2216***d*, **3016***a*, **3016***b*, **3016***c*, **3116***a*, **3116***b*, **3116***c*, **3216***a*, **3216***b*, **3216***c*, **4016***a*, **4016***b*, **4016***c*, **4116***a*, **4116***b*, **4116***c*, **4216***a*, **4216***b*, **4216***c*, **5016***a*, **5016***b*, **5016***c*, **5016***d*, **5016***e*, **5116***a*, **5116***b*, **5116***c*, **5116***d*, **5116***e*, **5116***f*, **6016***a*, **6016***b*, **6016***c*, **6016***d*, **6016***e*, **6016***f*, **6016***g* aperture
[0348] **1017***a*, **1017***b* organic semiconductor layer
[0349] **1018** passivation film
[0350] **1019***a*, **1019***b*, **2019***a*, **2019***b*, **2019***c*, **2019***d*, **2119***a*, **2119***b*, **2119***c*, **2119***d*, **2219***a*, **2219***b*, **2219***c*, **2219***d*, **3019***a*, **3019***b*, **3019***c*, **3019***d*, **3119***a*, **3119***b*, **3119***c*, **3119***d*, **3219***a*, **3219***b*, **3219***c*, **3219***d*, **4019***a*, **4019***b*, **4019***c*, **4019***d*, **4119***a*, **4119***b*, **4119***c*, **4119***d*, **4219***a*, **4219***b*, **4219***c*, **4219***d*, **5019***a*, **5019***b*, **5019***c*, **5119***a*, **5119***b*, **5119***c*, **5119***d*, **6019***a*, **6019***b*, **6019***c*, **6019***d*, **6019***e*, **6019***f* liquid-philic layer
[0351] **1132** color filter
[0352] **1133** black matrix
[0353] **10160** photoresist material film
[0354] **10170***a*, **10170***b* organic semiconductor ink

1. A thin-film transistor device comprising:

a first thin-film transistor element and a second thin-film transistor element that are arranged so as to be adjacent to each other with a gap therebetween, wherein

each of the first thin-film transistor element and the second thin-film transistor element comprises:

a gate electrode;

an insulating layer disposed on the gate electrode;

a source electrode and a drain electrode disposed on the insulating layer, the source electrode and the drain electrode being disposed with a gap therebetween;

a semiconductor layer disposed on the source electrode and the drain electrode so as to cover the source electrode and the drain electrode and fill the gap between the source electrode and the drain electrode, and being in contact with the source electrode and the drain electrode; and

a liquid-philic layer disposed on the insulating layer and having higher liquid philicity than the insulating layer, the liquid-philic layer being separate from the source electrode and the drain electrode, wherein

the thin-film transistor device further comprises partition walls disposed on the insulating layer and partitioning the semiconductor layer of the first thin-film transistor element from the semiconductor layer of the second thin-film transistor element, the partition walls having liquid-repellant surfaces and defining a first aperture, a second aperture, and a third aperture,

the first aperture surrounds at least a part of each of the source electrode, the drain electrode, and the liquid-philic layer of the first thin film transistor element,

the second aperture is adjacent to the first aperture and surrounds at least a part of each of the source electrode, the drain electrode, and the liquid-philic layer of the second thin film transistor element,

the third aperture is adjacent to the first aperture with a gap therebetween and is located in a direction, from the first aperture, differing from a direction of the second aperture,

an area of the thin-film transistor device surrounded by the third aperture does not include a semiconductor layer and does not function as a channel portion of the thin-film transistor device,

a bottom portion of each of the first and second apertures includes a source electrode portion being a bottom portion of the source electrode, a drain electrode portion being a bottom portion of the drain electrode, and a liquid-philic layer portion being a bottom portion of the liquid-philic layer,

in plan view, at the bottom portion of the first aperture, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the third aperture, and

in plan view, at the bottom portion of one of the first and second apertures, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the other one of the first and second apertures.

2. The thin film transistor device of claim **1**, wherein

the bottom portion of the first aperture includes a first portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer of the first thin film transistor element is in direct contact with the semiconductor layer of the first thin film transistor element, the first portion being within an area of the bottom portion located in the direction of the third aperture.

3. The thin film transistor device of claim **2**, wherein

the bottom portion of the first aperture further includes a second portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer of the first thin film transistor element is in direct contact with the semiconductor layer of the first thin film transistor element, the second portion being within an area of the bottom portion located in a direction differing from the direction of the third aperture, and

in plan view of the bottom portion of the first aperture, an area of the first portion is greater than an area of the second portion.

4. The thin film transistor device of claim **1**, wherein

in plan view, at the bottom portion of the other one of the first and second apertures, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the one of the first and second apertures.

5. The thin film transistor device of claim **1**, wherein

in plan view of the first, second, and third apertures,

the third aperture, the first aperture, and the second aperture are arranged in series in the stated order along a predetermined direction,

at the bottom portion of the first aperture, the center of area of the liquid-philic layer portion is offset from the center of area of the bottom portion in a first direction that intersects the predetermined direction, and

at the bottom portion of the second aperture, the center of area of the liquid-philic layer portion is offset from the center of area of the bottom portion in a second direction that intersects the predetermined direction.

6. The thin film transistor device of claim **5**, wherein

the first direction and the second direction are opposite directions.

7. The thin film transistor device of claim **1**, wherein

in each of the first and second thin film transistor elements,

the liquid-philic layer is formed by using a same material as used for forming the source electrode and the drain electrode, and

the liquid-philic layer is located apart from each of the source electrode and the drain electrode.

8. The thin film transistor device of claim **1**, wherein

in plan view of the bottom portions of the first and second apertures,

at the bottom portion of each of the first and second apertures, a center of area of each of the source electrode portion and the drain electrode portion coincides with the center of area of the bottom portion.

9. The thin film transistor device of claim **1**, wherein

in plan view of the bottom portions of the first and second apertures,

at the bottom portion of the first aperture, a center of a total of areas of the source electrode portion, the drain electrode portion, and the liquid-philic layer portion is offset from the center of area of the bottom portion in a direction differing from the direction of the third aperture, and

at the bottom portion of the second aperture, a center of a total of areas of the source electrode portion, the drain electrode portion, and the liquid-philic layer portion is offset from the center of area of the bottom portion in a direction differing from the direction of the first aperture.

10. The thin film transistor device of claim **1**, wherein

at the bottom portion of the first aperture,

a side of the liquid-philic layer portion located in the direction of the third aperture is located apart from a side surface portion, of the partition walls, facing the first aperture, and

a side of the liquid-philic layer portion located in a direction differing from the direction of the third aperture is in contact with the side surface portion, of the partition walls, facing the first aperture.

11. The thin film transistor device of claim **1**, wherein

a liquid repellency of the surfaces of the partition walls is greater than a liquid repellency of a surface of the insulating layer, in each of the first and second thin film transistor elements, that is in contact with the semiconductor layer, and

the liquid repellency of the surface of the insulating layer, in each of the first and second thin film transistor elements, that is in contact with the semiconductor layer is greater than a liquid repellency of a surface of each of the source electrode, the drain electrode, and the liquid-philic layer in each of the first and second thin film transistor elements.

12. The thin film transistor device of claim 1, wherein
a bottom portion of the third aperture includes a wire for electrically connecting with one of the source electrode and the drain electrode in the first thin film transistor element or one of the source electrode and the drain electrode in the second thin film transistor element.

13. An organic EL display element comprising:
the thin film transistor device of claim 1;
a planarizing film formed above the thin film transistor device and having a contact hole formed therein;
a lower electrode formed on the planarizing film so as to cover the planarizing film and a side surface of the planarizing film defining the contact hole, and electrically connected with one of the source electrode and the drain electrode in the first thin film transistor element or one of the source electrode and the drain electrode in the second thin film transistor element;
an upper electrode formed above the lower electrode; and
an organic light-emitting layer interposed between the lower electrode and the upper electrode, wherein
the contact hole is in communication with the third aperture of the thin film transistor device.

14. An organic EL display device comprising the organic EL display element of claim 13.

15. A method of manufacturing a thin film transistor device comprising:
forming a first gate electrode and a second gate electrode on a substrate so as to be adjacent to each other with a gap therebetween;
forming an insulating layer so as to cover the first gate electrode and the second gate electrode;
forming first and second source electrodes, first and second drain electrodes, and first and second liquid-philic layers on the insulating layer, wherein (i) the first source electrode and the first drain electrode are formed with respect to the first gate electrode with a gap therebetween, (ii) the second source electrode and the second drain electrode are formed with respect to the second gate electrode with a gap therebetween, (iii) the first liquid-philic layer is formed with respect to the first source electrode and the first drain electrode so as to be located apart from the first source electrode and the first drain electrode, the first liquid-philic layer having higher liquid philicity than the insulating layer, and (iv) the second liquid-philic layer is formed with respect to the second source electrode and the second drain electrode so as to be located apart from the second source electrode and the second drain electrode, the second liquid-philic layer having higher liquid philicity than the insulating layer;
depositing a layer of photosensitive resist material such that, above the insulating layer, the layer of photosensitive resist material covers the first and second source electrodes and the first and second drain electrodes as well as areas therearound;
forming partition walls on the insulating layer by performing mask exposure and patterning of the layer of photosensitive resist material, the partition walls having liquid-repellant surfaces and defining a first aperture, a second aperture that is adjacent to the first aperture, and a third aperture, the first aperture surrounding at least a part of each of the first source electrode, the first drain electrode, and the first liquid-philic layer, the second aperture surrounding at least a part of each of the second source electrode, the second drain electrode, and the second liquid-philic layer; and
forming a first semiconductor layer with respect to the first aperture and a second semiconductor layer with respect to the second aperture by applying semiconductor material with respect to the corresponding aperture and drying the semiconductor material so applied, wherein (i) the first semiconductor layer is formed so as to be in contact with the first source electrode and the first drain electrode, and (ii) the second semiconductor layer is formed so as to be in contact with the second source electrode and the second drain electrode, wherein
the partition walls are formed such that
the third aperture is adjacent to the first aperture with a gap therebetween and is located in a direction, from the first aperture, differing from a direction of the second aperture,
a bottom portion of each of the first and second apertures includes a source electrode portion being a bottom portion of the corresponding source electrode, a drain electrode portion being a bottom portion of the corresponding drain electrode, and a liquid-philic layer portion being a bottom portion of the corresponding liquid-philic layer,
in plan view, at the bottom portion of the first aperture, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the third aperture, and
in plan view, at the bottom portion of one of the first and second apertures, a center of area of the liquid-philic layer portion is offset from a center of area of the bottom portion in a direction differing from a direction of the other one of the first and second apertures.

16. The method of claim 15, wherein
the forming, on the insulating layer, of the first and second source electrodes, the first and second drain electrodes, and the first and second liquid-philic layers includes sub-steps of:
forming a metal layer on the insulating layer; and
etching the metal layer so formed.

17. The method of claim 15, wherein
the partition walls are formed such that the bottom portion of the first aperture includes a first portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer is to come in direct contact with the first semiconductor layer, the first portion being within an area of the bottom portion located in the direction of the third aperture.

18. The method of claim 17, wherein
the partition walls are formed such that the bottom portion of the first aperture further includes a second portion where the source electrode portion, the drain electrode portion, and the liquid-philic layer do not exist and thus, where the insulating layer is to come in direct contact with the first semiconductor layer, the second portion being within an area of the bottom portion located in a direction differing from the direction of the third aperture, and
in plan view of the bottom portion of the first aperture, an area of the first portion is greater than an area of the second portion.

19. The method of claim **15**, wherein

the forming of the insulating layer, the forming of the first and second source electrodes, the first and second drain electrodes, and the first and second liquid-philic layers, the forming of the partition walls, and the forming of the first and second semiconductor layers are performed such that

a liquid repellency of the surfaces of the partition walls is greater than a liquid repellency of a surface of the insulating layer that is to come in contact with the first and second semiconductor layers, and

the liquid repellency of the surface of the insulating layer is greater than a liquid repellency of a surface of each of the first and second source electrodes, each of the first and second drain electrodes, and each of the first and second liquid-philic layers.

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专利名称(译)	薄膜晶体管器件及其制造方法，有机电致发光显示元件和有机电致发光显示器件		
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摘要(译)

薄膜晶体管元件形成在由分隔壁限定的第一孔和第二孔中的每一个中，其进一步限定第三孔，第三孔与第一孔相邻，其间具有间隙，并且位于从第一孔开始的方向上，不同于第二孔的方向。在平面图中，在第一孔的底部，亲液层部分的区域的中心在不同于第三孔的方向的方向上偏离底部的区域的中心，并且在第一和第二孔中的一个的底部，亲液层部分的区域的中心在与第一和第二孔中的另一个的方向不同的方向上偏离底部的区域的中心。